A Modular Re-Programmable Digital Receiver Architecture

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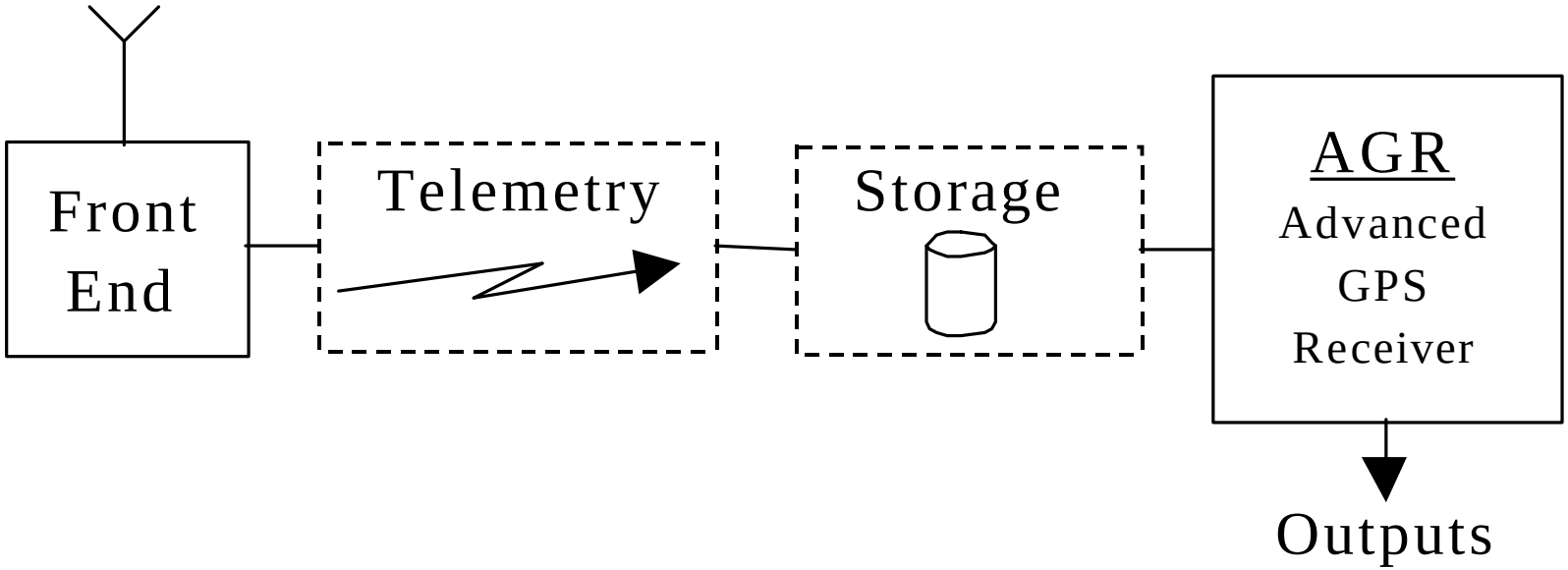
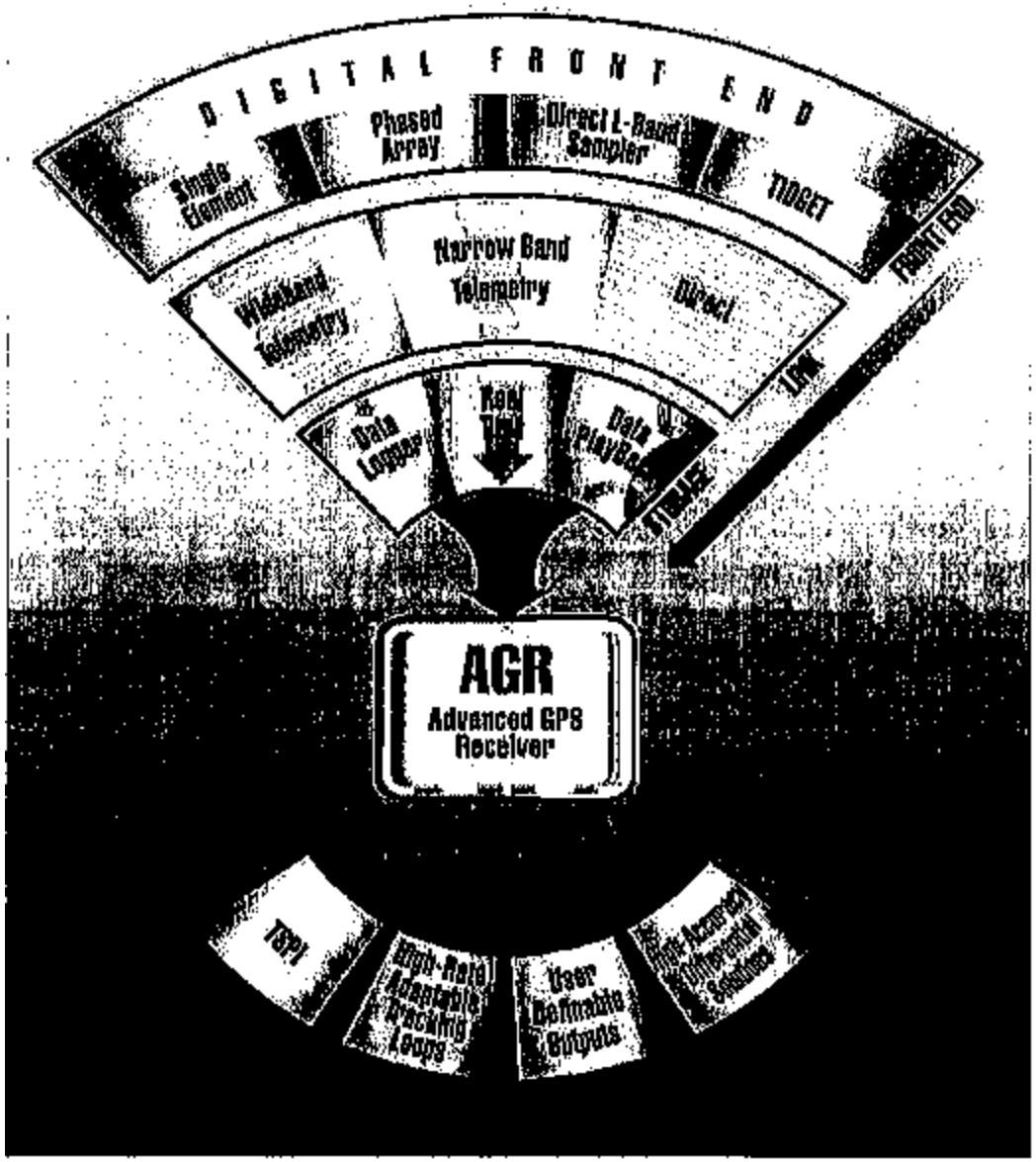
Modular Receiver Architecture



Options for the Modular Receiver Architecture



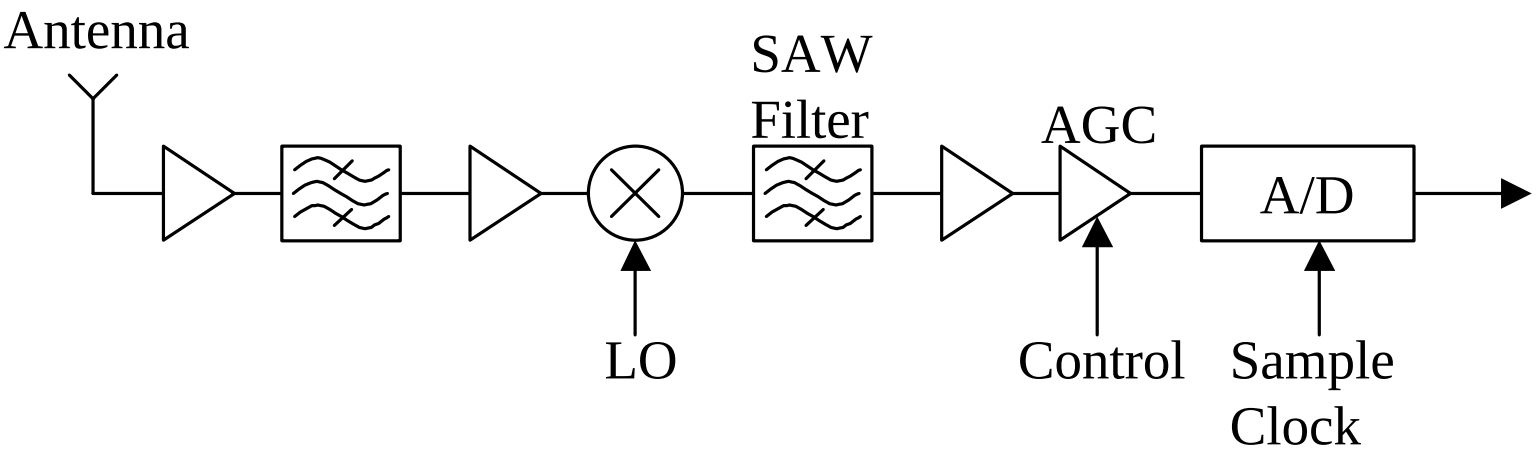
AGR Performance Specifications

Frequency	L1, 1575.42 MHz
Code	CA Code
Channels	8 Channels
Correlator Spacing	Adjustable
Dynamics	
Velocity	10,000 m/s
Acceleration	100 g
Jerk	100 g/s
Data Output Rate	1 - 1000 Sample/s
Time To First Fix	40 sec (cold - no time or position)
Re-Acquisition	10 sec to valid position
Nominal Signal Level	-136 to -86 dBm
Digital Samples	I, Q, or I&Q
A/D resolution	1 - 4 bits
Sample Rate	2 - 25 MHz

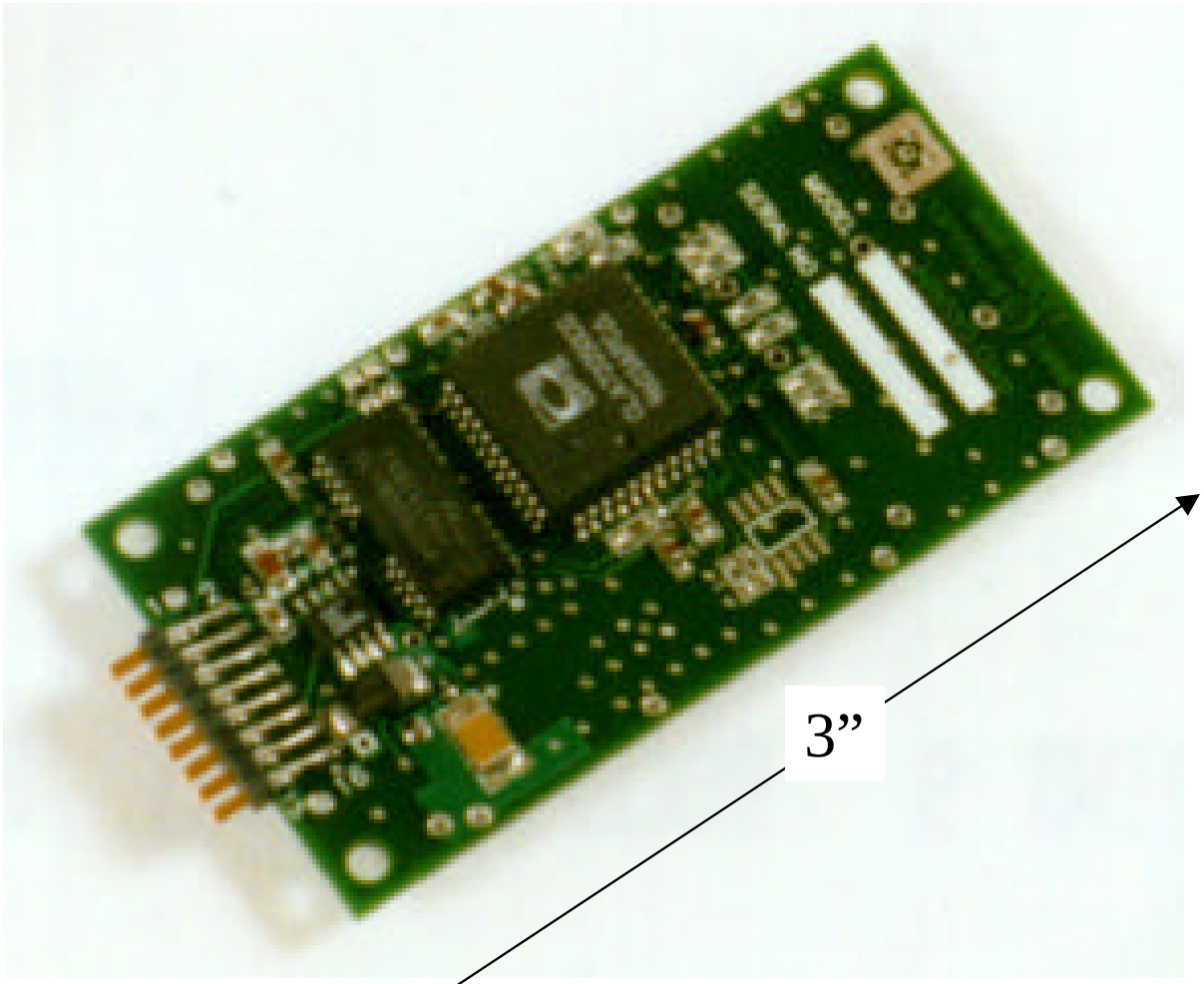
AGR Configuration Parameters

- Dynamics
- Bandwidths for Delay-Lock Loop / Phase-Lock Loop / Frequency-Lock Loop
- Track Thresholds
- DFE Characteristics
- Correlator Spacing
- Data Logging Rates
- Satellite Selection Methods

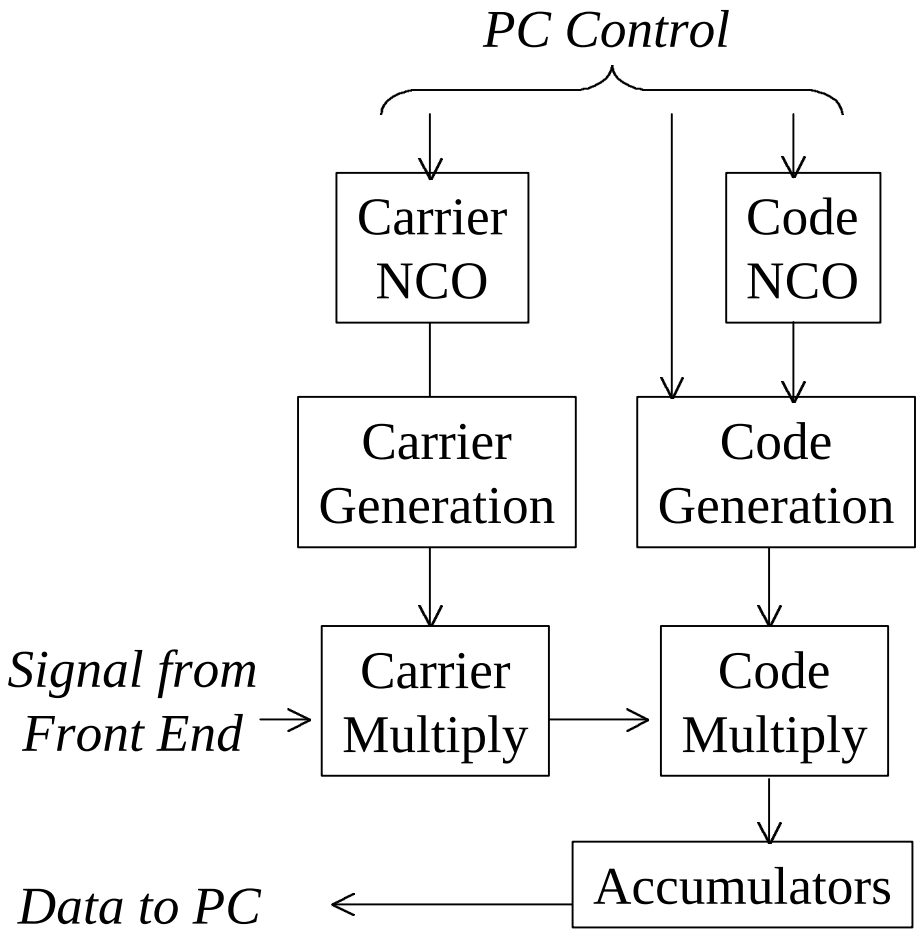
Basic Digitizing Front End Architecture



TIDGET Digitizing Front End



Correlator Accelerator Card



Ruggedized AGR

MATLAB Simulation