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DSP Architectures for Wireless
Communications

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Agenda

♦ Current State of the Phone
  ✤ Architecture
  ✤ Implementation
  ✤ Power

♦ Future Trends
  ✤ 3rd Generation Requirements
  ✤ Application Trends
  ✤ Impact on Architectures
Complete Digital Engine ON A Single Chip

- .18 um Timeline™ ASIC design methodology
- TMS320C54x wireless-optimized DSP core
- Low-power ARM7TDMI microcontroller core
- Dual core co-emulation speeds development time
- Available system software modules
- Flexibility allows platform reuse across standards
GSM Baseband Cellular Architecture

Digital Baseband

Analog Baseband
Task Partitioning

Host
- Man-Machine Interface
- User Applications
- Data Exchange
- Data Processing
- Internet Access

Interface
- Shared Memory
- Parallel
- Serial Peripheral
- Custom

DSP
- Communications
- Speech I/O
- GPS
- Audio
- Video
- Security
Handset Power Breakdown

GSM Handset Power Breakdown - EFR : Class 5 (0.8W)

GSM EFR Class 5

1997

60%  
13%  
27%

Digital BB □ Analog BB ■ RF

GSM EFR Class 5

2000

81%  
17%  
2%

Digital BB □ Analog BB ■ RF
Viterbi Accelerator

- Compare, Select, and Store Unit (CSSU) for Viterbi Algorithm
  - Two 16b ADD/SUB operations in single cycle
  - Store max value and update state history in single cycle
Peripherals: Buffered Serial Port

- Based on serial port
- High speed data transfers
- Reduced Interrupt Latencies
- Read/Write to 2K words Ram
- CPU not burdened
Peripherals: Host Port Interface

- 8 bit parallel port
- Interfacing MCU
- Shared DARAM
  2K Word Memory
- SAM Mode:
  - DSP and MCU
  - 64MBps @ 40 MHz
- HOM Mode:
  - DSP and MCU
  - 160 MBps @ 40 MHz
- IDLE2
Power Dissipation

- **Mechanisms to Lower Power**
  - Bus Keepers / Holders - maintain state of external. Bus
  - External Bus off control - disables the external bus
  - Static design - lower clock to DC
  - IDLE 1, 2, 3, modes - drop into various power down modes
  - PLL options (31 options on C548) - use lower system clock
  - MIPS efficiency - fewer MIPS enables
Power Dissipation

◆ IDLE Modes

◆ IDLE1 7.93mA for IDLE1 (3V/66mips)
  – Turns off clocks to the process core
  – Clocks to peripherals remain active

◆ IDLE2 2mA for IDLE2 (3V/66mips)
  – Turns off clocks to the process core and to some peripherals
  – Clocks to BSP and HPI remain active

◆ IDLE3 1uA for IDLE3 (3V/66mips)
  – Turns off clocks to the process core, to all peripherals and halts PLL
1 Volt DSP For Wireless

- 63 MHz operation at 1V, 100 MHz at 1.35V
- 15x power improvement over existing technology (3.3V)
Frequency Vs. Supply Voltage

- 63 MHz at 1.0V, 100 MHz at 1.35V
- 15x power improvement over existing technology (3.3V)
Power Vs. Frequency

- 17 mW at 1V and 63 MHz
- 19x improvement in mW/MHz
- 15x reduction in power at 60 MHz
Energy Delay Product

- Minimum at 1.0V

![Graph showing Energy-Delay Product vs Supply Voltage (V)]

- X-axis: Supply Voltage (V)
Future - Terminals

♦ Data will surpass voice for wireless demand
  ✿ Killer App not yet identified

♦ Power
  ✿ Standby/Talk times equivalent to cordless needed.
  ✿ Standby times measured in weeks, talk times high enough that battery never goes dead.
Future - Terminals - Cont.

♦ Open platforms
  - More 3rd parties developing software
  - HLL/RTOS support in DSP/MCU
  - CACHE or RAM based processing predominant

♦ Standards
  - 3G will drive MIPS required into 1000s of MIPS range
Future - Terminals

Applications
- Echo cancellation/Voice Dialing - Safety of Use
- Video
- Navigation
- E911
- TBD
Wireless Processing Requirements

- GSM
- IS-95
- IS-136+
- W-TDMA
- W-CDMA

MIPS

MCU
DSP
ASIC
Speech Recognition

DSP Core
S/W

Speech Recognition

Microcontroller Core
S/W

SINGLE CHIP DIGITAL BASEBAND
Wireless Watchdog

NURSERY

ZOOM IN
ZOOM OUT
PAN LEFT
PAN RIGHT
SWITCH CAMERAS
Bibliography

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