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FPGAs: Enabling the Software/Reconfiguable Radio
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DSP Chief Architect


Agenda
• Device Technology
• Software
• Design Methodologies
• Example
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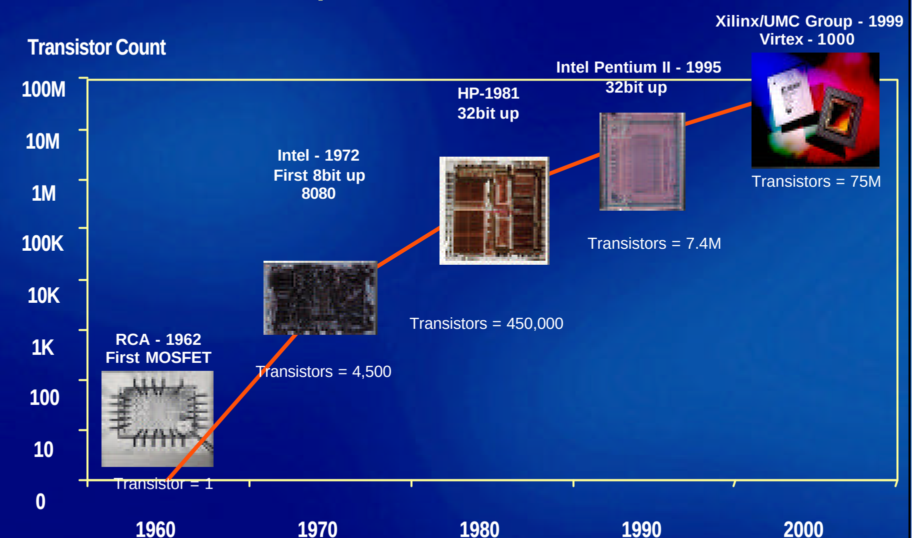
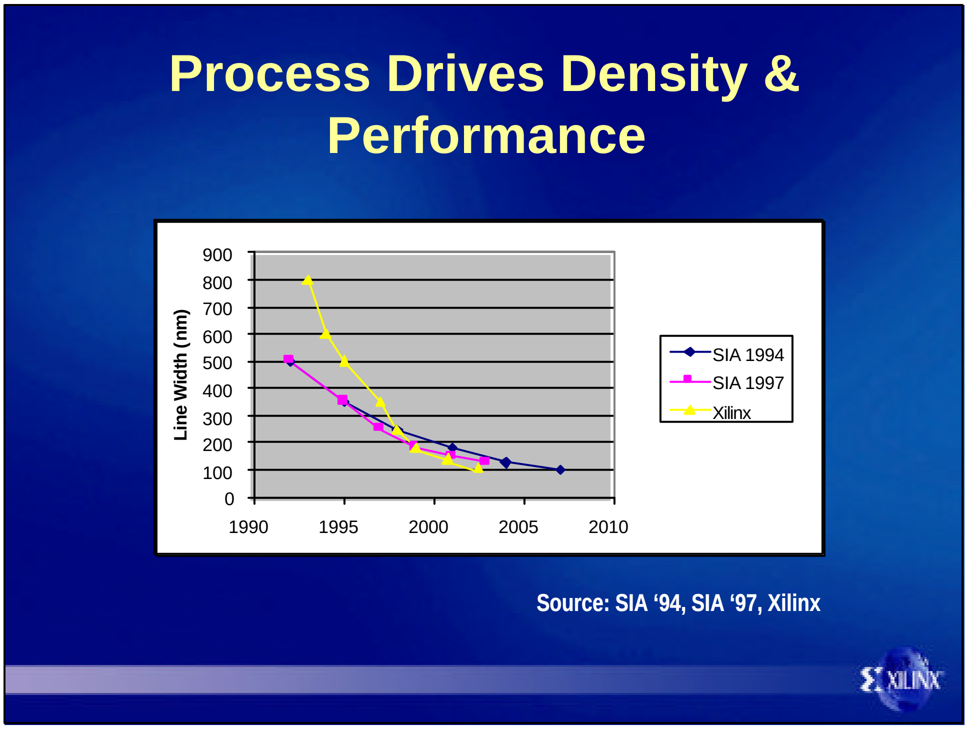
Why FPGA DSP?

- Flexibility
- High performance
- Time to Market
- Functional extensions to existing equipment
- Standard part (no NRE/Inventory issues)
- Early system bring-up on hardware

The Impact of Moore's Law




Process Drives Density & Performance
900
800
700
600
500
400
300
200
100
0
Line Width (nm)
1990
1995
2000
2005
2010
SIA 1994
SIA 1997
Xilinx
Source: SIA '94, SIA '97, Xilinx
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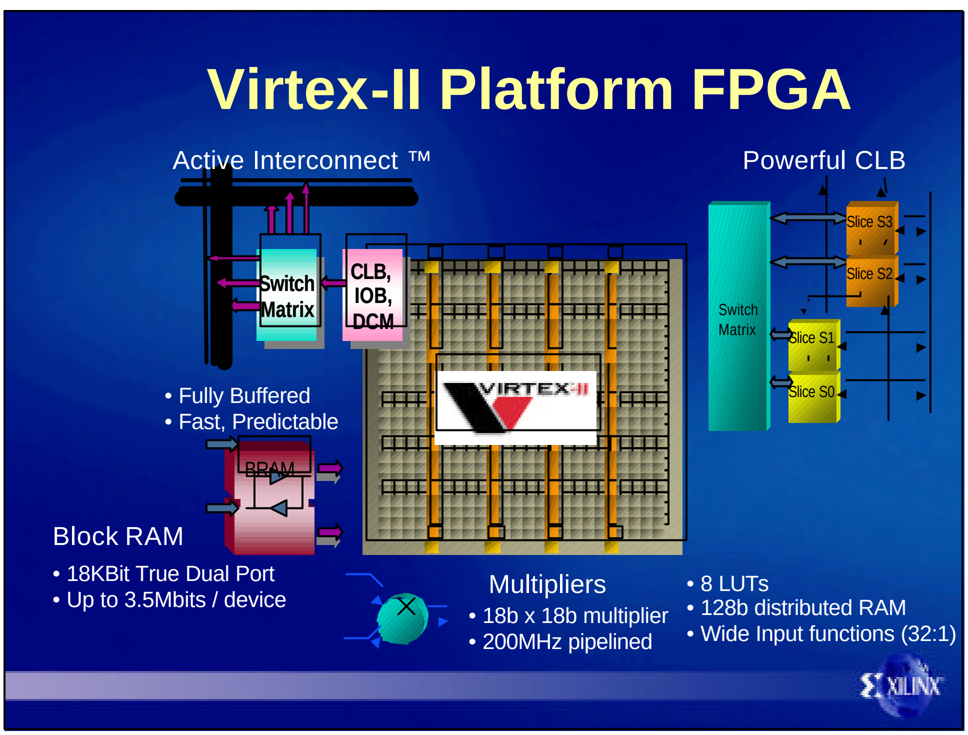
Virtex-II Platform FPGA
Active Interconnect ™
Switch Matrix
CLB, IOB, DCM
• Fully Buffered
• Fast, Predictable
BRAM
Block RAM
• 18KBit True Dual Port
• Up to 3.5Mbits / device
VIRTEX-II
Powerful CLB
Switch Matrix
Slice S3
Slice S2
Slice S1
Slice S0
Multipliers
• 18b x 18b multiplier
• 200MHz pipelined
• 8 LUTs
• 128b distributed RAM
• Wide Input functions (32:1)
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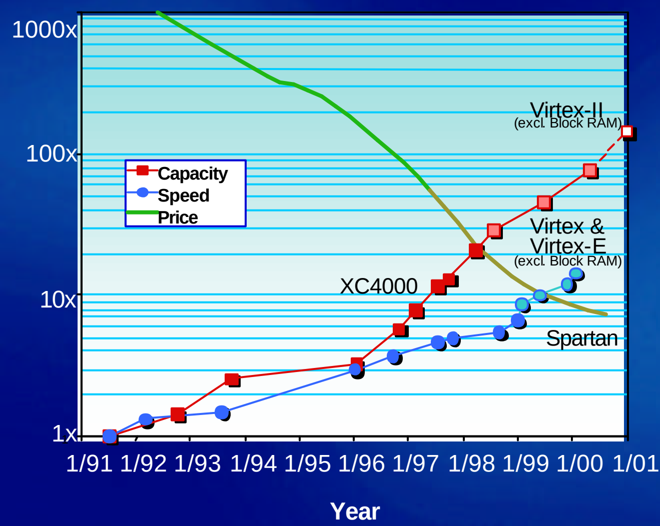
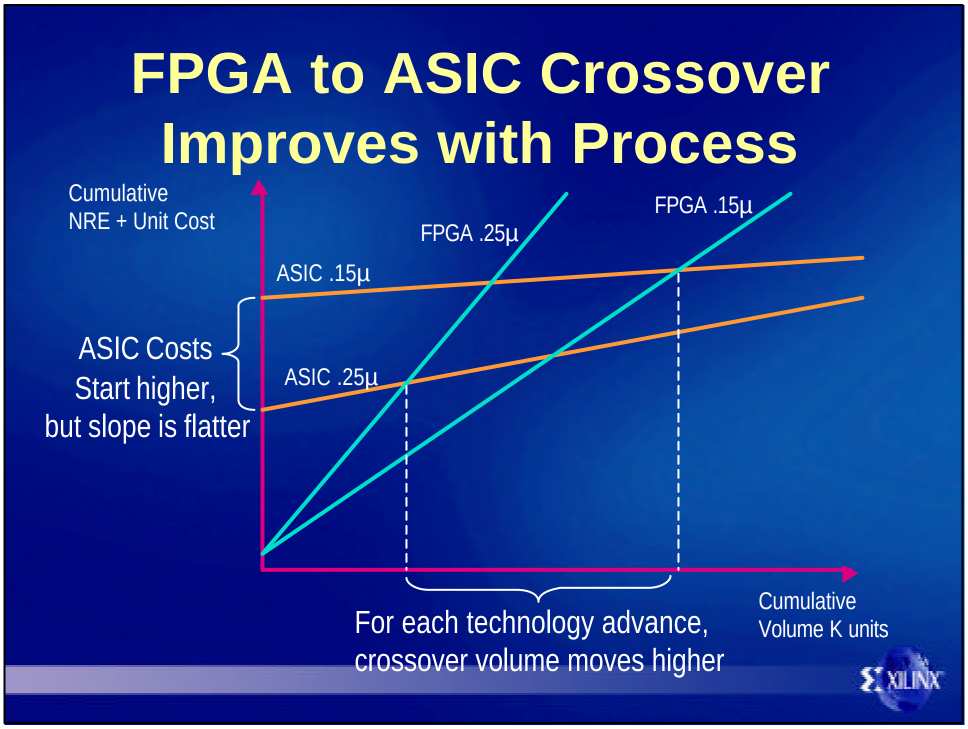
A Decade of Progress



Virtex®-II Family

Virtex-II Part Number	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
Logic Cells	576	1152	3456	6912	11520	17280	24192	32256	51840	76032	104832
BRAM (Kb)	72	144	432	576	720	864	1008	1728	2160	2592	3024
Multipliers	4	8	24	32	40	48	68	96	120	144	168
DCM Units	4	4	8	8	8	8	8	12	12	12	12
CS144	88	92	92								
FG256	88	120	172	172	172						
FG456			200	264	324						
FG676						392	456	484			
FF896					432	528	624				
FF1152								720	824	824	824
FF1517									912	1104	1108
BG575					328	392	408				
BG728							456	516			
BF957							624	684	684	684	684

11 Devices, 10 Packages, 37 combinations



FPGA to ASIC Crossover
Improves with Process
Cumulative
NRE + Unit Cost
FPGA .25µ
FPGA .15µ
ASIC .15µ
ASIC Costs
Start higher,
but slope is flatter
ASIC .25µ
For each technology advance,
crossover volume moves higher
Cumulative
Volume K units
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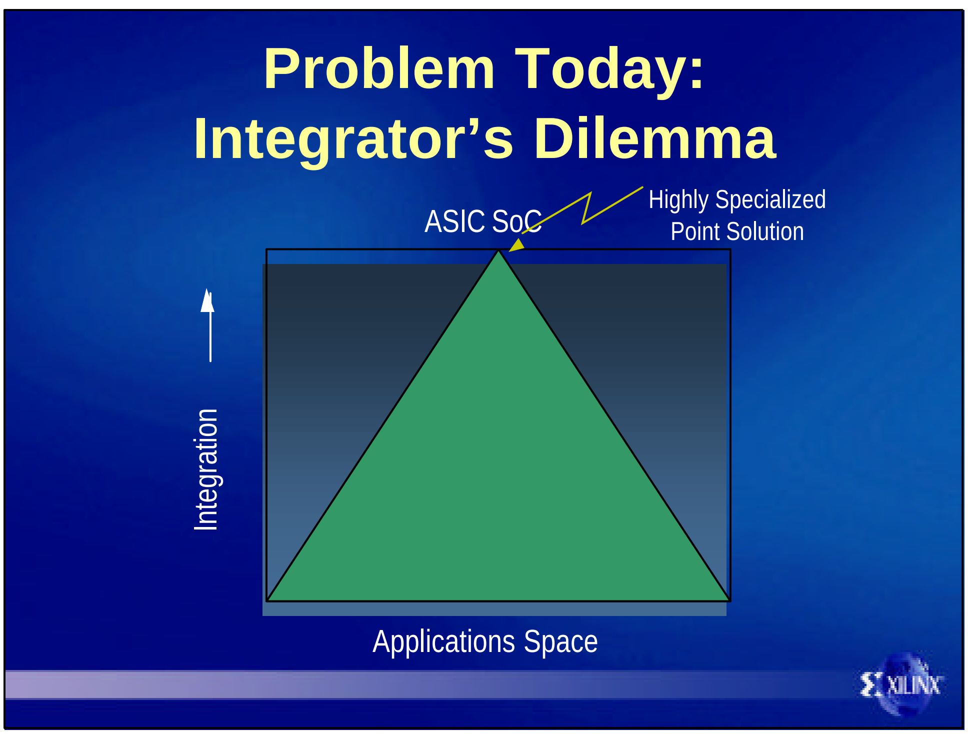

Problem Today:
Integrator's Dilemma
ASIC SoC
Highly Specialized
Point Solution
Integration
Applications Space
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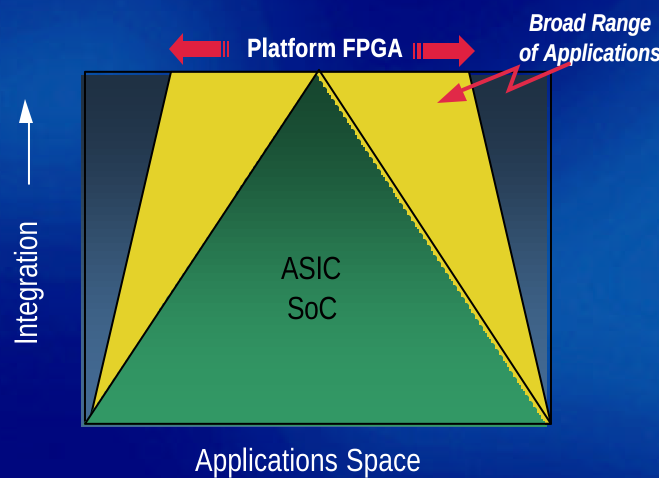
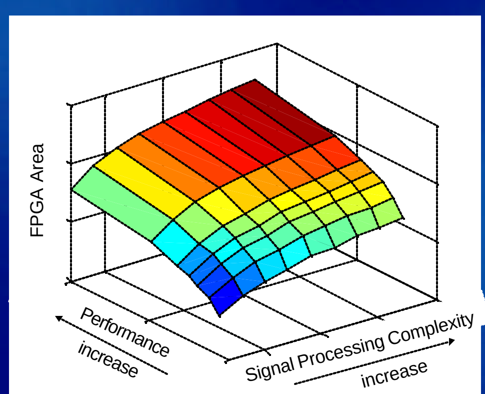
New Era of Platform FPGAs



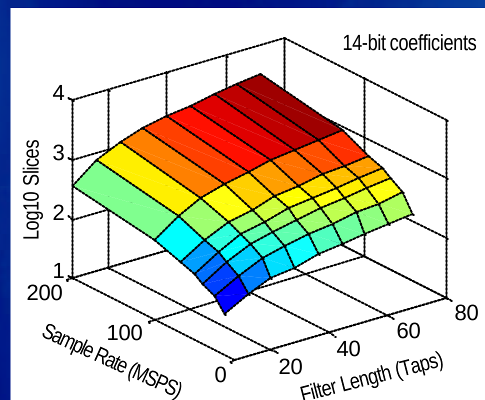
FPGA Customized Datapaths

- Design tradeoffs and optimization in real (design)-time



Example: FIR Filter

- Use optimum precisions at each node in the computation graph
- 'Right-size' the datapath
- design surface for a FIR filter: Area vs Sample Rate vs Length



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Adding Parallelism in Conventional DSP Solutions

- New DSP architectures such as VLIW and super-scalar have one goal: provide higher degrees of parallelism
- Architecture evolution along the same design axis is not scalable
  - Too many MAC functional units makes programming, compilers and scheduling an issue
- The effective computing per chip area decreases
  - Memories grow geometrically while the datapath does not

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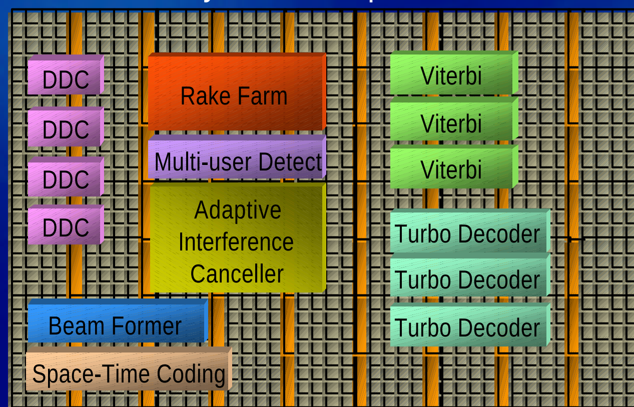
The Power of Parallelism

- In FPGAs we can exploit the large amounts of parallelism inherent in many DSP data paths



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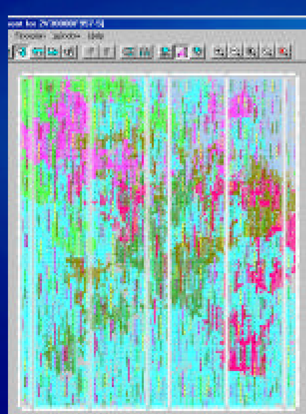
FPGAs = Performance (1)



- 12 concurrently operating 64-tap filters
- 8-bit MACs – 8-bit data, 8-bit coefficients†
- Sample Rate (fs) = 154 MHz
- 13,704 slices (95% of device)
- 118 Billion MACs/s
- I/O bandwidth = 237 Giga-bytes/s

Virtex-II XC2V3000-5 with 14,336 slices

† Optimized for coefficient set

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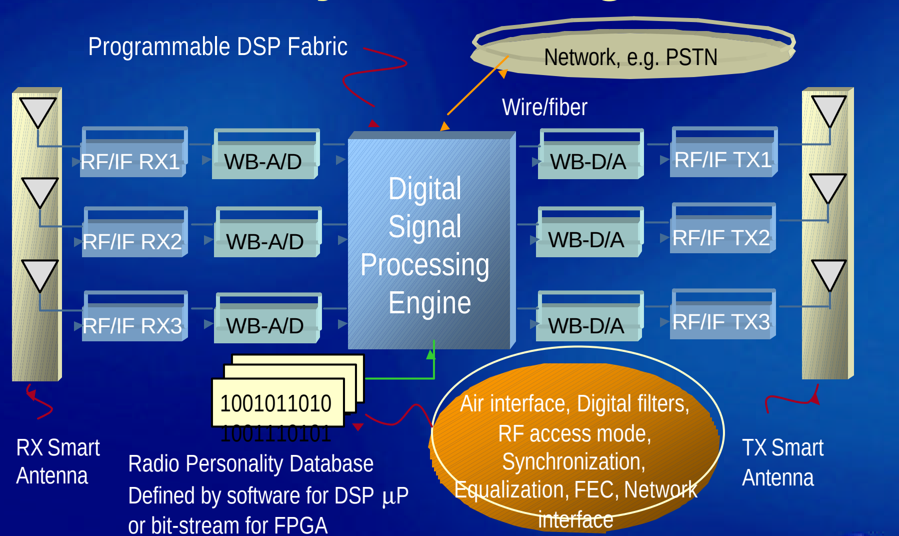
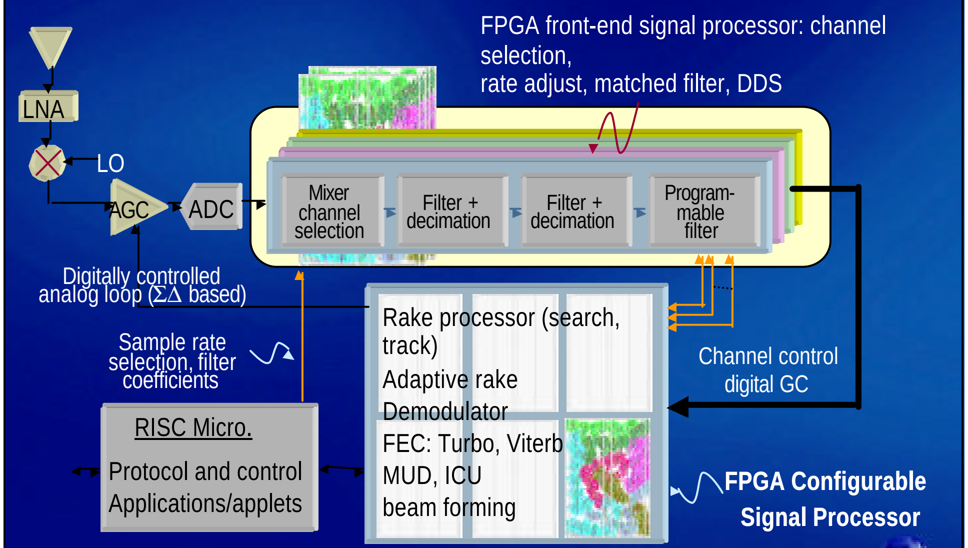
FPGAs = Performance (2)

- 1024-point complex FFT
  - 9 microsecond execution time (@fclk = 115 MHz)
  - 2,500† logic slices
- Viterbi decoder at OC3 data rates: 155 Mbps
- Interleaver/de-interleaver @fclk > 200 MHz
- RS decoding @10 Gbps
  - 16 parallel RS decoders in a single XC2V3000-4

SDR System Diagram



Wideband BTS - Receiver



Building the System

- Device technology is part of the solution
- The software/IP is getting harder than the hardware
- Design methodologies for
  - Productivity
  - Rapid design exploration
  - Hardware abstraction
  - Single source for all aspects of the design & development cycle
    - Verification
    - Implementation

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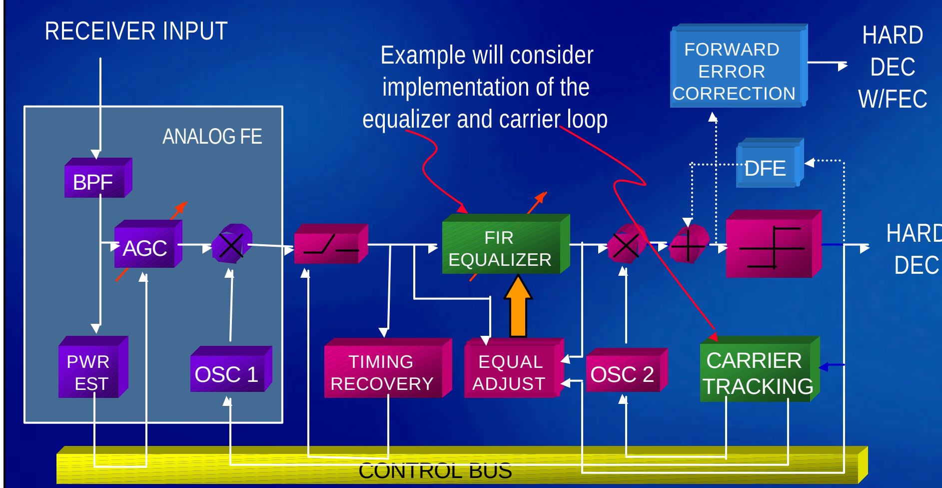
SDR Personality: QAM Receiver



The Design Space is Rich

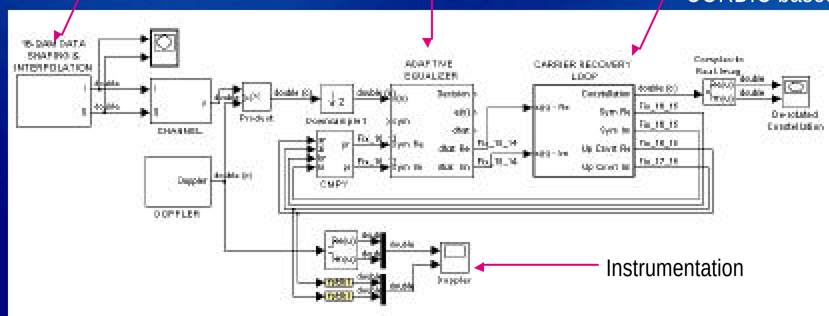
- Decision directed T/2 Adaptive Equalizer - LMS based update
- Using FPGAs There are multiple architectural choices available to meet a desired area/performance objective
- Fully parallel
  - N MAC processing elements (PEs)
  - N LMS PEs
- Folded architecture
  - 1 MAC PE & 1 LMS PE for each polyphase segment
- … Many others

Equalized Receiver Example

Transmitter Model
- 16-QAM Source
- Matched Filter
- Sample rate Change

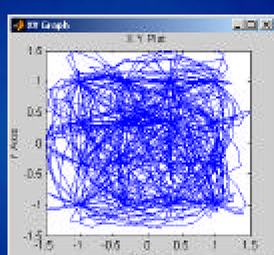
Passband Adaptive Equalizer
- Fractionally spaced (T/2)
- Polyphase decimator structure
- LMS coefficient update
- coefficients updated at the symbol rate

Carrier Recovery
- CORDIC based PD

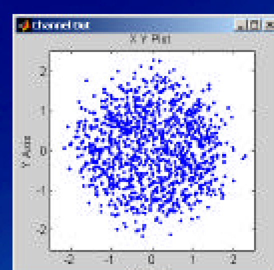


System Generator Simulation

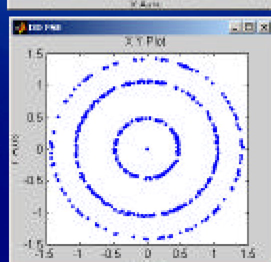
TX const. Transition diagram



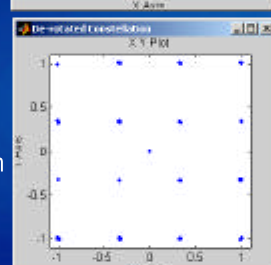
Rx signal with ISI & Doppler



Equalized No carrier lock



Equalized constellation

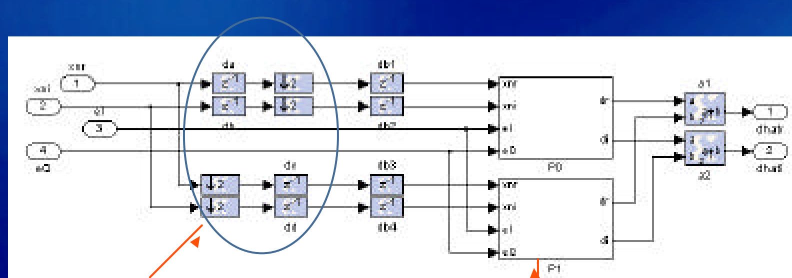


Implementation

- Parallel T/2 FSE
- Polyphase decomposition
- 8-taps total
  - 4 taps in each polyphase segment
- 8-LMS PEs
- Coefficients updated at the symbol rate

Pipelined Parallel T/2 DD FSE

- Design components are based on a library of highly optimized module generators

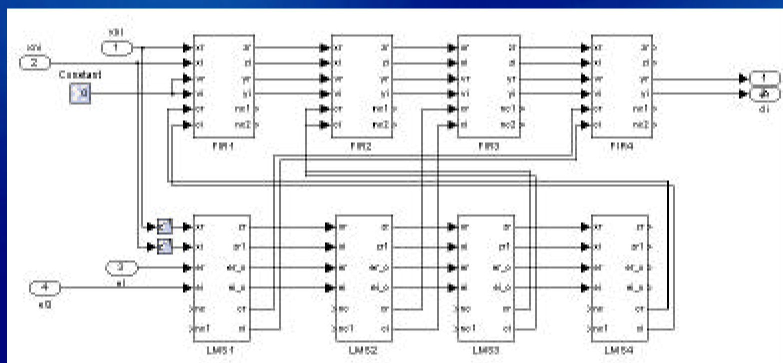


Input sample commutator

Polyphase Filter produces samples at the symbol rate

Pipelined Parallel T/2 FSE

- One polyphase segment
  - 4 FIR PEs & 4 LMS PEs



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Pipelined Parallel T/2 FSE

- Design statistics for 8 tap equalizer
  - 2674 logic slices
  - 66 multipliers
    - 64 used for FIR + LMS PEs, 2 for rate adaption
  - fclk = 149.5 MHz (-6 speed grade part)
- Computation rate: 9.6 Giga-MACs

† software version 4.1.03i, speedfile version 1.93, par -rl 5 -pl 5 -xe 2

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Folded FSE

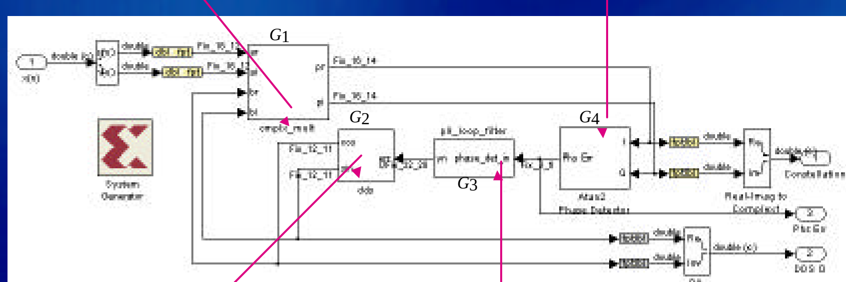
- Benchmark data
  - 2093 logic slices
  - 16 embedded multipliers
  - fclk † = 100 MHz (XC2V3000bf957-6)
- For fclk = 100 MHz and N=8 T/2 FSE the symbol rate is 25 Msym/s
- For 16-QAM this is 100 Mbps

† software version 4.1.03i, speedfile version 1.93, par -rl 5 -pl 5 -xe 2

Carrier Recovery Loop

Mixer using Virtex-II
Embedded multipliers
- 3 multipliers/ 5 additions

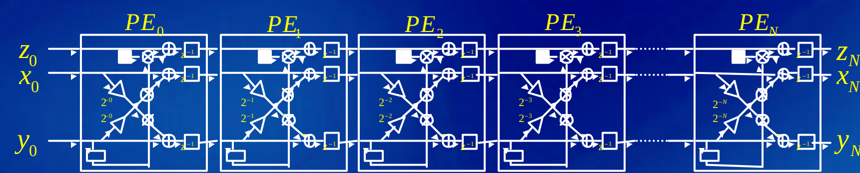
CORDIC based
phase detector

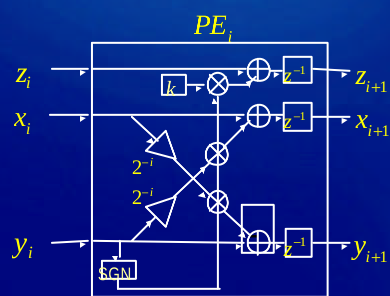


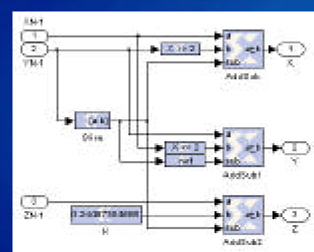
Look-up table Based DDS

PI Loop filter using 2
embedded multipliers

CORDIC Phase Detector







System Generator Implementation

CRL Resources

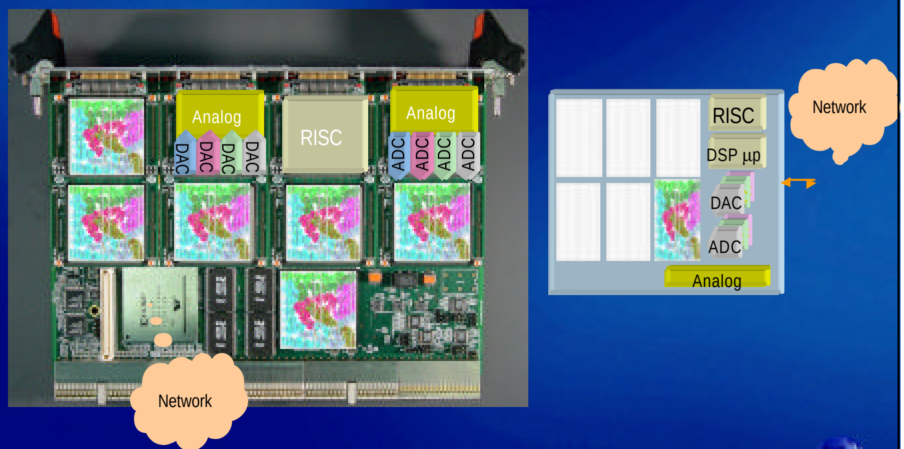
Function	Slice Count	Block RAMs	Embedded Multipliers
Heterodyne	111	-	3
DDS	5	1	-
Loop Filter	32	-	2
Phase Detector	270	-	3

Total	413†	1	8

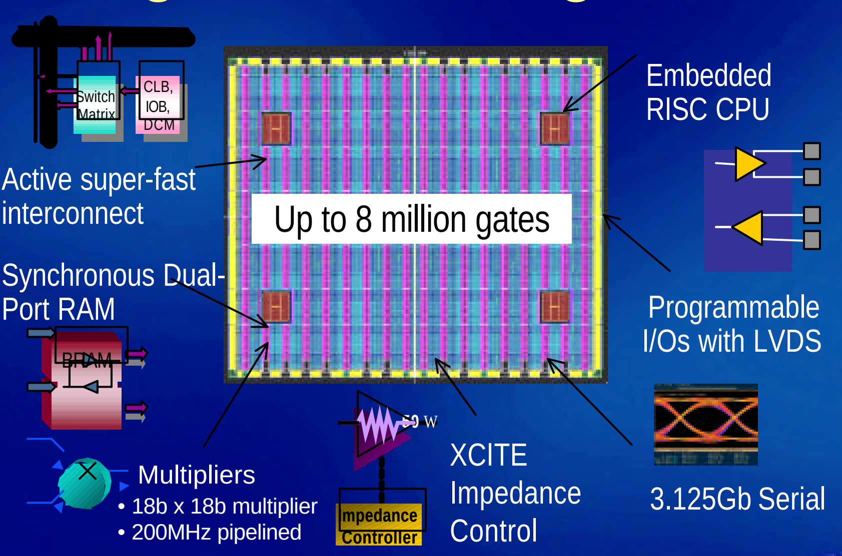
† The small slice count discrepancy is due to logic optimizations that occur when the individual CRL components are integrated into the complete system.)

DIME - Modular System Building

Board image courtesy of Nallatech http://www.nallatech.com/

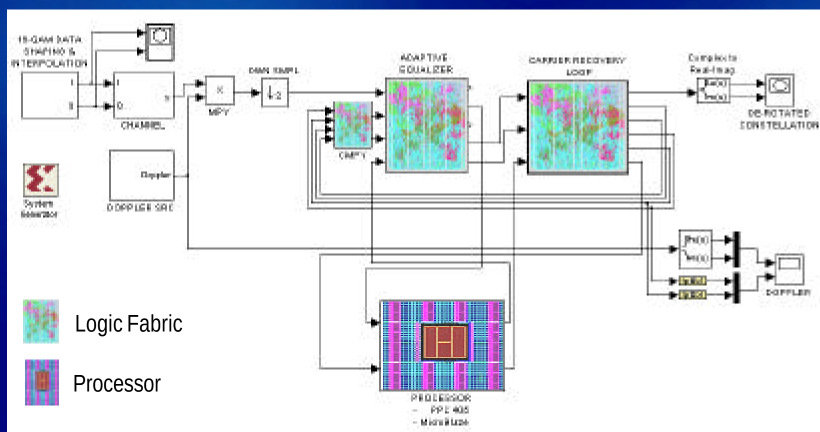


The Signal Processing Platform



Platform Based Design

- Hardware/Software partitioning



The Future

- Trends
  - Increasing levels of System integration
  - Pervasive DSP enabling anywhere anytime connectivity
  - Increasingly complex systems
  - Decreasing market windows
- FPGA DSP systems
  - Device technology supporting highly parallel DSP engines
  - Design methodologies
    - Abstraction that permits working in the language of the problem
    - Enables effective integration of re-usable components (cores)