Spectrum Monitoring with UAS

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Outline

- UAS Overview
- Constrained SWaP Hardware
- Processing Package Hierarchy
- Hardware Package 1: Data Recorder
- Hardware Package 2: SoC FPGA Accelerated
- Hardware Package 3: Embedded Processing
- Conclusion
UAS Overview: Why Fly?

• Spatial diversity
  – Cover a wide geographic area rapidly
  – Cover otherwise impassible terrain
  – Estimate emitter location

• Altitude diversity
  – Clear structures, trees, or obstacles
  – Increase visible horizon
  – Variation in received power
    • Transmitter elevation pattern
    • Multipath propagation

• Overcome path loss

<table>
<thead>
<tr>
<th>Range</th>
<th>Center Frequency</th>
<th>R² Path Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 km</td>
<td>915 MHz</td>
<td>91.7 dB</td>
</tr>
<tr>
<td>1 km</td>
<td>2.45 GHz</td>
<td>100.3 dB</td>
</tr>
<tr>
<td>1 km</td>
<td>5.8 GHz</td>
<td>107.8 dB</td>
</tr>
</tbody>
</table>
UAS Overview: Fixed Wing

Advantages

• Hardware integration space
• Higher payload weight
• Longer endurance
• Antenna integration space
• Fast flight
• Can be robust to weather

Disadvantages

• Constant motion
• Bank in turns
• Aerodynamics must be considered for antennas
• STOL
• Typically for outdoor use
UAS Overview: Skywalker X8

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Endurance</td>
<td>30 minutes</td>
</tr>
<tr>
<td>Cruising Speed</td>
<td>30 mph (GS)</td>
</tr>
<tr>
<td>Range</td>
<td>15 miles (linear)</td>
</tr>
<tr>
<td>Altitude</td>
<td>0-400 ft. AGL</td>
</tr>
<tr>
<td>Size</td>
<td>6.95 ft. wingspan</td>
</tr>
<tr>
<td>Payload Capacity</td>
<td>3 lbs.</td>
</tr>
<tr>
<td>Power</td>
<td>LiPo</td>
</tr>
<tr>
<td>Platform Cost</td>
<td>$500</td>
</tr>
<tr>
<td>Recurring Cost</td>
<td>Battery Recharge</td>
</tr>
</tbody>
</table>
UAS Overview: Multirotor

Advantages

• Small and maneuverable
• Loiter in a hover
• Tight pointing control
• Indoor or outdoor
• VTOL

Disadvantages

• Limited payload size/weight
• Limited endurance
• Rotating props can affect antenna patterns
• Limited antenna placements
• Less robust to weather
UAS Overview: AlienCopter Bee

- **Endurance**: 15 minutes
- **Cruising Speed**: 15 mph (GS)
- **Range**: 3.75 miles (linear)
- **Altitude**: 0-400 ft. AGL
- **Size**: 2.2 ft. prop-prop
- **Payload Capacity**: < 1.9 lbs.
- **Power**: LiPo
- **Platform Cost**: $650
- **Recurring Cost**: Battery Recharge
UAS Overview: Weather Balloon

Advantages

• Extremely high altitude
• Long endurance
• Capable of lifting large, heavy payloads

Disadvantages

• No control
• Limited launch windows
• Restrictions on launch locations
• Equipment must be hardened for near-space conditions
UAS Overview: EoSS Enclosure

**Platform Overview**

- **Endurance**: 4 hours
- **Cruising Speed**: N/A
- **Range**: N/A
- **Altitude**: 0-90 kft. AGL
- **Size**: 1 ft. x 1 ft. x 1 ft.
- **Payload Capacity**: < 5 lbs.
- **Power**: USB Battery Pack
- **Platform Cost**: $10
- **Recurring Cost**: ~$300/flight

Launch services provided by Edge of Space Sciences: www.eoss.org
UAS Overview: Common Avionics

- Pixhawk autopilot and uBlox GPS
  - $290 for both
- PX4 firmware stack
- Provides blended navigation solution
- Wide variety of platforms supported
- Several built-in flight control modes
- ROS or mavlink libraries used for interfacing
- Subscribe to:
  - GPS with QoS
  - Orientation in Euler angles or Quaternions
  - Local position estimates

Image from: www.pixhawk.org
Constrained SWaP Hardware

- Each platform has constraints on the size, weight, and power of equipment it can support (SWaP)
- Power provided by modern LiPo batteries is abundant
  - AlienBee battery provides >300 W
- Space for electronics integration is limited
- Payload weight is extremely limited
  - Additional payload directly impacts flight time/range
SDR Hardware

Radio Front End
- Frequency Conversion
- Conditioning
- Data conversion

Programmable Logic
- Custom logic circuits
- Low latency
- Highly parallel
- Limited memory
- Rigidly defined
- Long compile times

General Purpose Processor
- Flexible software
- Open-source tools
- Fast clocks
- Access to RAM and HD
- Networked

Physical Connection

High Speed Bus

Network Connection
SDR Hardware Implications

- Power limitations preclude the sustained use of high power amplifiers for transmission
- Size and weight restrictions limit the choice of processing hardware
  - PCIe cards and ATX motherboards are too bulky
  - GPUs are typically too heavy
- Embedded single-board-computers (SBCs) are small enough
- FPGAs are small and highly efficient
  - Leverage the existing programmable logic in the SDR architecture
Historical Embedded Limitations

- SBCs have historically suffered from:
  - Low performance CPUs
    -> Limits proc. rate
  - Small amount of RAM
    -> Limits buffer sizes
  - Slow interfaces (USB 2.0, UART)
    -> Limits radio peripheral data rates
  - Slow memory hardware (SD cards)
    -> Limits full rate data recording
Enabling Technologies

- **Smart phones**
  - Faster, multi-core CPUs
  - More RAM
  - High performance interface support
  - Wide bandwidth memory support

- **FPGAs and Moore’s law**
  - Faster, cheaper, smaller

- **System-on-chips**
  - Integrates FPGA/CPU
  - Reduces package size
  - High rate data interface

- **Radio-on-chips (RF ICs)**
  - Ultra-low SWaP
Processing Hierarchy

- Hierarchy of processing established to address SWaP constrained challenges
- Increasing algorithm maturity
- Increasing on-board processing
- Increasing development time/effort
- Decreasing flexibility
Processing Hierarchy

1. Data Recorder
   a. Low performance CPU
   b. High rate memory interface
   c. No guidance feedback
   d. Ideal for algorithm development
   e. Processing is all off-line
   f. Fly, record, land, process, update
Processing Packages: Data Recorder

HackRF One Radio

HummingBoard SBC

- Used in field deployment
- Used for data offloading

rtl-SDR

USB 2.0

WiFi

256 GB SSD

MSata

Ethernet

Image from: www.mathworks.com
## Processing Packages: Data Recorder

<table>
<thead>
<tr>
<th>CPU Cores</th>
<th>CPU Clock</th>
<th>Interfaces</th>
<th>RAM</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.2 GHz</td>
<td>USB 2.0, Ethernet, mPCIe</td>
<td>1 GB</td>
<td>32 GB SD, 256 GB SSD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FPGA Name</th>
<th>FPGA Cells</th>
<th>FPGA BRAM</th>
<th>FPGA Multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Radio Name</th>
<th>Channel</th>
<th>Duplex</th>
<th>IBW</th>
<th>Freq. Range</th>
<th>Bits</th>
<th>Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>HackRF</td>
<td>1 Rx/TX</td>
<td>Half</td>
<td>&lt;20 MSPS</td>
<td>1 MHz - 6 GHz</td>
<td>8</td>
<td>USB 2.0</td>
</tr>
<tr>
<td>rtl-SDR</td>
<td>1 Rx</td>
<td>N/A</td>
<td>&lt;2.4 MSPS</td>
<td>24 MHz-1766 MHz</td>
<td>8</td>
<td>USB 2.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Size</th>
<th>Weight</th>
<th>Power</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1&quot; x 4.9&quot; x 1.6&quot;</td>
<td>0.39 lbs.</td>
<td>6.5 W</td>
<td>$475</td>
</tr>
</tbody>
</table>
Processing Packages: Data Recorder

- Separate IQ data and metadata recording
- Take metadata with ROS or library plug-ins
- User Google protocol buffers for metadata
  - Time-stamp
  - Radio state
  - GPS
  - Local position estimate
  - Orientation
  - Air-data
  - File-name, offset, size

- IQ Data is large
  - 8 bits @ 2 MSPS => 3.8 MB/s
  - 16 bits @ 20 MSPS => 76 MB/s
  - 2x 16 bits @60 MSPS => 458 MB/s

- Protobuf metadata is used to index
  - Raw parsing
  - SQLite database

- Avahi networking is used to connect data recorder to ground-station in the field

- Ethernet is prefered for data transfers in the lab
Hardware Packages and Results

Processing Packages: Data Recorder

- Initial version of data recorder was integrated with DJi Phantom 2
- rtl-SDR radio was integrated
  - Directional log-periodic antenna
- GPS only
- HD could record ~16 hours of IQ data at 2.4 MSPS
- Circular flight plan was executed
- Altitude varying flight plan was executed
  - Leverage variation in el. patterns
- GPS tagged results were used to generate heat-maps
  - User visualization
  - Coverage maps
  - Emitter Localization

Scan Results

Frequency: 900 to 917.875

Coverage map and heat-map visualization.
Hardware Packages and Results

- Lessons learned from first flight were adapted, package was upgraded
- Two packages were integrated into a weather balloon
  - HackRF radios
  - One duck antenna, one log-period
- One package scanned TV bands
  - Looking to estimate HDTV antenna elevation patterns
- One package linearly scanned through bands
- Pixhawk with PX4 was integrated
  - ROS used for integration
- Protobufs included in data recording
- HDTV package could record IQ data for ~6 hours at 6 MSPS
- Scanning package could record IQ data for ~4 hours at 10 MSPS

94,000 ft apogee

~63 mile cross-range drift

Our github for this project: github.com/dirkcgrunwald/ros-sdr
Processing Packages: Data Recorder

617 MHz
Processing Packages: Data Recorder

515 MHz
Processing Packages: Data Recorder

549 MHz
Processing Hierarchy

2. Onboard CPU Processing
   a. High performance CPU
   b. High rate interfaces
   c. Guidance feedback possible
   d. Somewhat mature algorithms
   e. Processing can be distributed
   f. Software keeps it flexible
   g. Design algorithms for low processing
Processing Packages: Onboard CPU Processing

**Ettus B205mini**

**ODroid XU4**

- **USB 3.0**
- **WiFi** Used in field deployment
- **Ethernet** Used for data offloading

**128 GB SSD**
## Processing Packages: Onboard CPU Processing

<table>
<thead>
<tr>
<th>CPU Cores</th>
<th>CPU Clock</th>
<th>Interfaces</th>
<th>RAM</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>2 GHz</td>
<td>USB 2.0, USB 3.0, Ethernet</td>
<td>2 GB</td>
<td>32 GB SD, 64 GB eMMC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FPGA Name</th>
<th>FPGA Cells</th>
<th>FPGA BRAM</th>
<th>FPGA Multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan 6 LX150</td>
<td>147k</td>
<td>4824 Kb</td>
<td>180</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Radio Name</th>
<th>Channels</th>
<th>Duplex</th>
<th>IBW</th>
<th>Freq. Range</th>
<th>Bits</th>
<th>Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9364</td>
<td>1 Rx/TX</td>
<td>Full</td>
<td>&lt;~30 MSPS</td>
<td>70 MHz - 6 GHz</td>
<td>12</td>
<td>USB 3.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Size</th>
<th>Weight</th>
<th>Power</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3” x 3.5&quot; x 2&quot;</td>
<td>0.23 lbs.</td>
<td>&lt;23 W</td>
<td>$889</td>
</tr>
</tbody>
</table>
Processing Packages: Onboard CPU Processing

- Lessons learned adopted
- Port selection is important
  - USB 3.0 shared by radio, Ethernet, and SSD
- Near continuous data recording
  - Buffer to bigger RAM
  - Write to eMMC/SSD
- No GNU Radio or ROS
  - Development overhead
  - More flexibility without
  - Adapt principles

- Choose the right language
  - Fast processing in C++
  - Complicated code in python
  - Protobufs for compatibility
- Processing integrated with ZMQ
  - Efficient and distributable
- Design algorithm to minimize processing
  - Log2 vs. Log10
  - Running max holds
Processing Packages:  
Onboard CPU Processing

- Signal identification application was developed
- Frequency-domain detection of PSD envelope using deep learning techniques
- Max-hold reduces data rate and maintains privacy
- Wideband data is collected in frequency and time
- Feeds trained 2D CNN
- CNN produces probability of label
- Front end, CNN, and visualization can be distributed
Processing Packages: Onboard CPU Processing

Git repo: bitbucket.org/austinsteamboat/cnn_sdr_specmon
Processing Hierarchy

3. Onboard FPGA Acceleration
   a. Host bulk of DSP on FPGA
   b. CPU for management
   c. Guidance feedback possible
   d. Very mature algorithms
   e. Firmware is rigidly designed
   f. Design algorithms for full-rate processing
Processing Packages: Onboard FPGA Acceleration

FMCOMMS3

Zedboard

FMC

Ethernet

Used for data offloading

FMCOMMS Image from: www.analog.com
Zedboard Image from: www.zedboard.org
## Processing Packages: Onboard FPGA Acceleration

<table>
<thead>
<tr>
<th>CPU Cores</th>
<th>CPU Clock</th>
<th>Interfaces</th>
<th>RAM</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>667 MHz</td>
<td>USB 2.0, Ethernet</td>
<td>512 MB</td>
<td>32 GB SD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FPGA Name</th>
<th>FPGA Cells</th>
<th>FPGA BRAM</th>
<th>FPGA Multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zynq 7Z020</td>
<td>85k</td>
<td>4480 Kb</td>
<td>220</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Radio Name</th>
<th>Channels</th>
<th>Duplex</th>
<th>IBW</th>
<th>Freq. Range</th>
<th>Bits</th>
<th>Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9361</td>
<td>2 Rx/TX</td>
<td>Full</td>
<td>2-61.44 MSPS (56 MHz max)</td>
<td>70 MHz - 6 GHz</td>
<td>12</td>
<td>FMC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Size</th>
<th>Weight</th>
<th>Power</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.3” x 9.4” x 0.9”</td>
<td>0.43 lbs.</td>
<td>7 W</td>
<td>$1069</td>
</tr>
</tbody>
</table>
Processing Packages: Onboard FPGA Acceleration

- SoCs result in very small packages
- Tight integration of CPU/FPGA simplifies high-rate data interface
- Zedboard has slow CPU, big FPGA
  - Host bulk of DSP in firmware
  - Let CPU manage
- Data is preprocessed to significantly reduce rate exposed to CPU

- Focus on developing modular, open-source designs
  - Improves design reusability
  - Easier for porting
- Network-on-Chip (NoC) architecture
  - Simplifies integration
  - Improves versatility of FPGA
- Automated Build tools
  - Reduces challenge of tool compatibility
Hardware Packages and Results

- Satellite navigation project at CU researching using signals of opportunity
- Extract timing from GPS disciplined ATSC signal
- FPGA design to:
  - Apply complex auto-correlation
  - Detect resulting peaks
  - Report power and timing of peaks
- Modular components were developed and implemented
- Reduces data rate from 23 MB/s to 0.48 KB/s
  - 50000x reduction in data rate
Processing Packages: Onboard FPGA Acceleration

- NoC architecture developed
- Standard interfaces
- Reconfigure processing chain
- AXI-4 stream and cross-bar switch
  - Simple
  - Widely compatible
- Supports asynchronous designs
- Automated build process for integrating computing elements
  - Uses python scripting for VHDL and TCL script generation
  - Uses Docker for tool stability
  - Launching as a web service

Git Repo: bitbucket.org/cusdr/cunoc_sdr/wiki/Home
Processing Packages: Onboard FPGA Acceleration
Processing Packages: Onboard FPGA Acceleration
Going Forward

- Separate CPU/FPGA
  - Fully leverage advances in embedded CPUs
- Focus on widely used OS with package manager
  - Software installation is a major challenge
  - The more its used, the more bugs are worked out
- Start flying more
  - New FAA regulations are far friendlier
Automating Spectrum Forensics
Anderson, et. al

Path Forward

Going Forward

Ettus B205mini

ODroid XU4

USB 3.0

USRP 3: B205 Firmware

User Firmware

Radio Phy

Data Framing

USB 3.0 Phy

LimeSDR

Sprite Drone

Modular Payload Bay

LimeSDR Image from: www.crowdsupply.com/lime-micro/limesdr
Sprite Image from: www.ascentaerosystems.com
Conclusion

• UAS are cost effective and practical
• UAS mobility improves spectrum monitoring performance
• SWaP drives hardware
• Embedded processors are getting better
• Hardware acceleration improves performance
  • Critical for full-rate processing
• Metadata database accelerates post-processing
• Design of efficient algorithms enables on-board processing
• Widely used SBCs reduce software development risks
• Separate FPGA and CPU improves flexibility
• FPGA development time can be reduced with NoC architecture
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- Tyler Clayton - RECUV
- Matt Busby - RECUV
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- Will Finamore – Aircraft Hardware Integration Engineer
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- Ryan Handzo – CU CCAR, ATSC Navigation Research
- Adam St. Amand - CU CCAR, ATSC Navigation Research
- Jorge Cervantes - CU CCAR, ATSC Navigation Research
- Donald Kuettel III - CU CCAR, ATSC Navigation Research
- Dr. Denis Akos – CU CCAR, GPS Interference Research
References


Backups
UAS Overview: Aerostat

Advantages
• Extremely long endurance
• Capable of lifting large, heavy payloads
• Very few regulations

Disadvantages
• No control
• Anchored in place
• Helium refills can be expensive over time
• Sensitive to inclement weather
### UAS Overview: Aerostat

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Endurance</strong></td>
<td>Days</td>
</tr>
<tr>
<td><strong>Cruising Speed</strong></td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Range</strong></td>
<td>Tethered</td>
</tr>
<tr>
<td><strong>Altitude</strong></td>
<td>0-165 ft. AGL</td>
</tr>
<tr>
<td><strong>Size</strong></td>
<td>20 ft. long, 700 cubic feet</td>
</tr>
<tr>
<td><strong>Payload Capacity</strong></td>
<td>14 lbs.</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>LiPo</td>
</tr>
<tr>
<td><strong>Platform Cost</strong></td>
<td>$1600</td>
</tr>
<tr>
<td><strong>Recurring Cost</strong></td>
<td>&gt;$100/flight</td>
</tr>
</tbody>
</table>

Image from: www.advertising-balloons.com
Motivating Case Study

- Interference detected in ATSC band during machine learning collections
- Source is narrow-band
- Intermittent in time
- Powerful
- Found to be TV white-space microphones
  - Used by distance learning courses at CU
Motivating Case Study

DTV Station KPJR-DT • Channel 38 • Greeley, CO
Expected Operation on June 13: Granted Construction Permit
Digital CP (solid): 1.20 kW ERP at 362 m HAAT
Market: Denver, CO

Coverage gained after DTV transition
Digital service 2,252,665 persons

Image from: www.fcc.gov
Motivating Case Study
Motivating Case Study
Motivating Case Study

• Localized, intermittent interference
  • Challenging for manual discovery
  • Well suited for automated UAS

• Interference source is asymmetric
  • Strong incentive for incumbent to take action

• FCC mapping provides insufficient guidance
  • Automated UAS can rapidly generate accurate, up-to-date radio maps