Spectrum Monitoring with UAS

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Outline

- **UAS Overview**
- **Constrained SWaP Hardware**
- **Processing Package Hierarchy**
- **Hardware Package 1: Data Recorder**
- **Hardware Package 2: SoC FPGA Accelerated**
- **Hardware Package 3: Embedded Processing**
- **Conclusion**

UAS Overview: Why Fly?

- Spatial diversity
  - –Cover a wide geographic area rapidly
  - –Cover otherwise impassible terrain
  - –Estimate emitter location
- Altitude diversity
  - –Clear structures, trees, or obstacles
  - –Increase visible horizon
  - –Variation in received power
    - Transmitter elevation pattern
    - Multipath propagation
- Overcome path loss

Range	Center Frequency	R^2 Path Loss
1 km	915 MHz	91.7 dB
1 km	2.45 GHz	100.3 dB
1 km	5.8 GHz	107.8 dB

UAS Overview: Fixed Wing

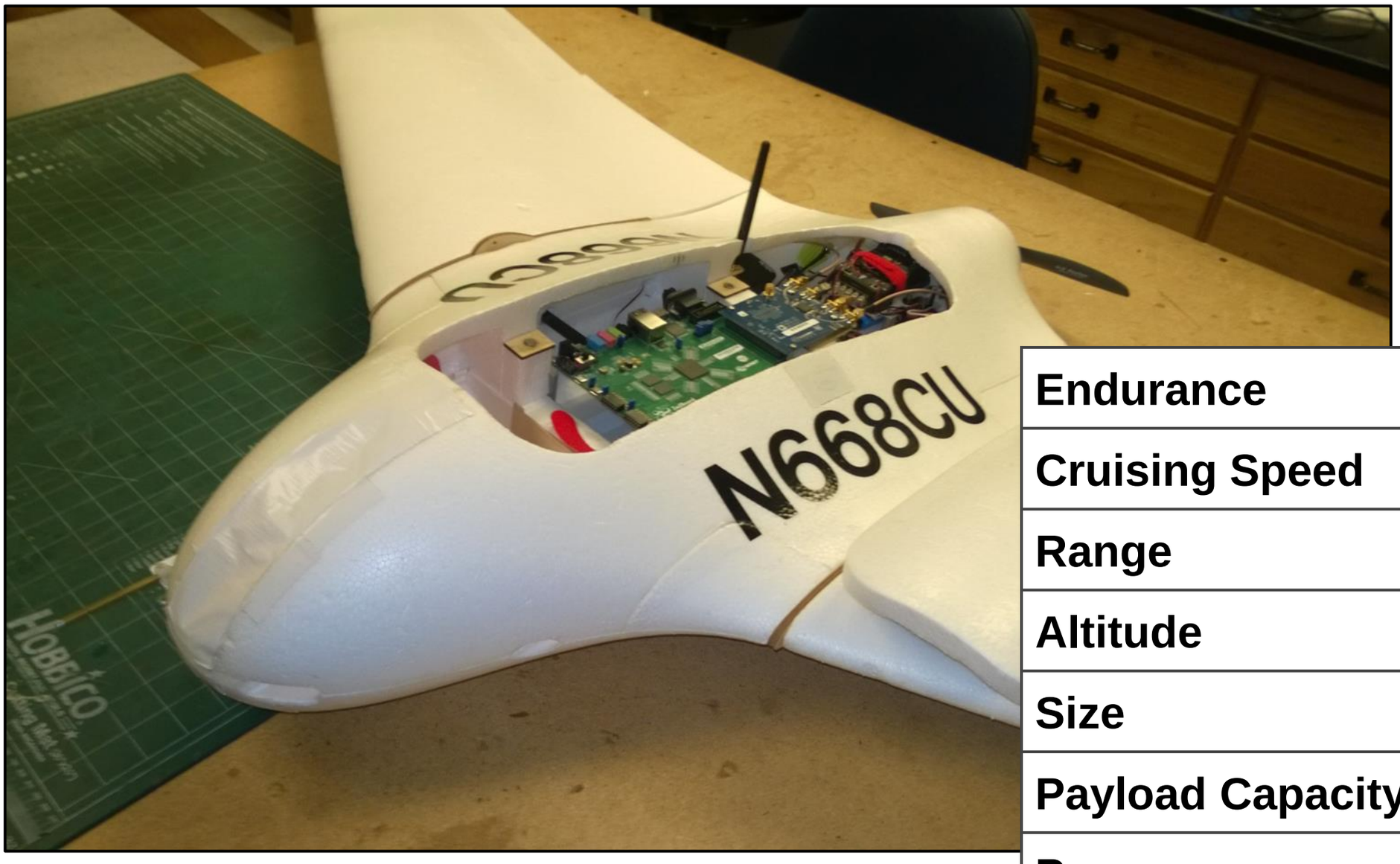
Advantages

- Hardware integration space
- Higher payload weight
- Longer endurance
- Antenna integration space
- Fast flight
- Can be robust to weather

Disadvantages

- Constant motion
- Bank in turns
- Aerodynamics must be considered for antennas
- STOL
- Typically for outdoor use

UAS Overview: Skywalker X8



Endurance	30 minutes
Cruising Speed	30 mph (GS)
Range	15 miles (linear)
Altitude	0-400 ft. AGL
Size	6.95 ft. wingspan
Payload Capacity	3 lbs.
Power	LiPo
Platform Cost	$500
Recurring Cost	Battery Recharge

UAS Overview: Multirotor

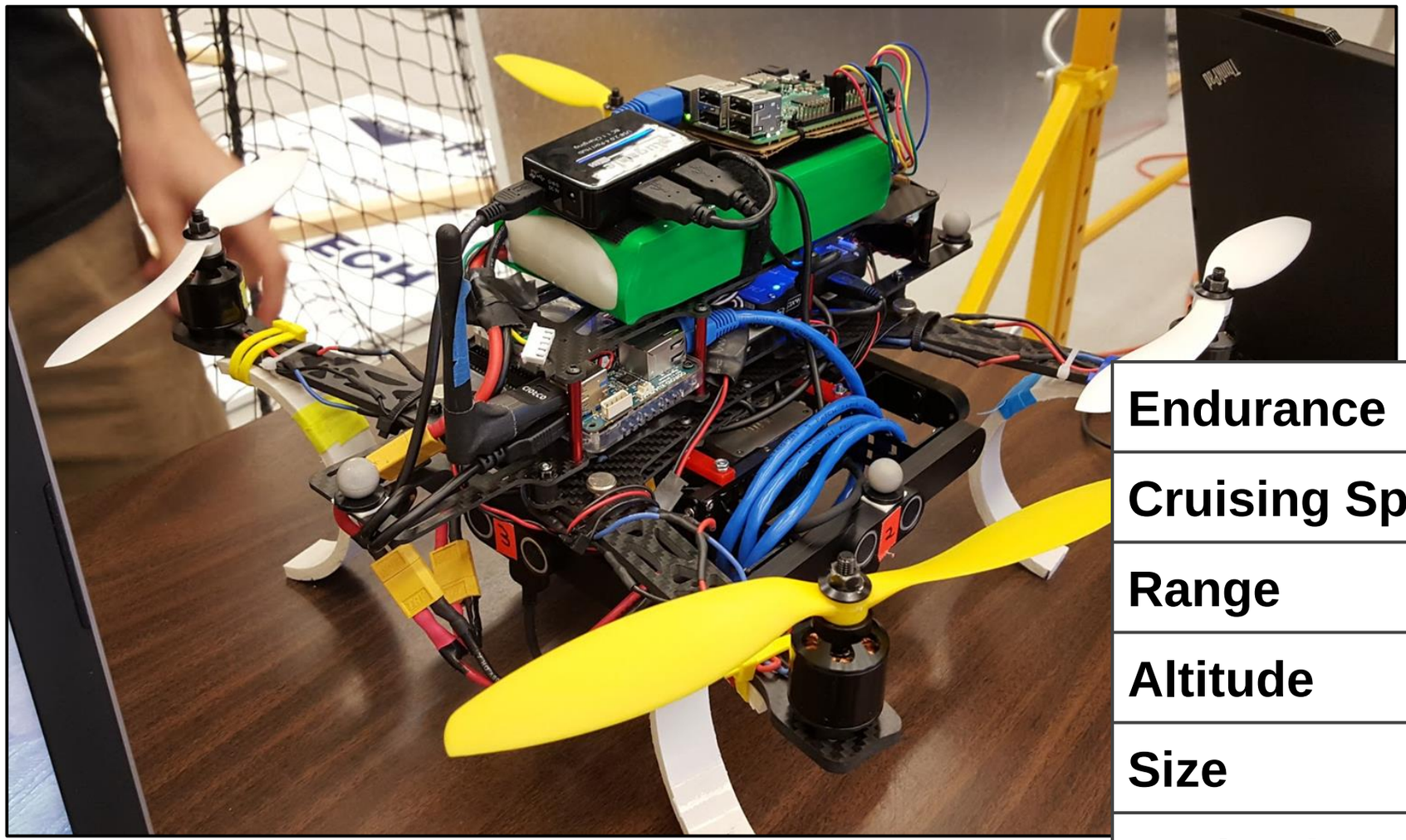
Advantages

- Small and maneuverable
- Loiter in a hover
- Tight pointing control
- Indoor or outdoor
- VTOL

Disadvantages

- Limited payload size/weight
- Limited endurance
- Rotating props can affect antenna patterns
- Limited antenna placements
- Less robust to weather

UAS Overview: AlienCopter Bee



Endurance	15 minutes
Cruising Speed	15 mph (GS)
Range	3.75 miles (linear)
Altitude	0-400 ft. AGL
Size	2.2 ft. prop-prop
Payload Capacity	< 1.9 lbs.
Power	LiPo
Platform Cost	$650
Recurring Cost	Battery Recharge

UAS Overview: Weather Balloon

Advantages

- Extremely high altitude
- Long endurance
- Capable of lifting large, heavy payloads

Disadvantages

- No control
- Limited launch windows
- Restrictions on launch locations
- Equipment must be hardened for near-space conditions

UAS Overview: EoSS Enclosure

Endurance	4 hours
Cruising Speed	N/A
Range	N/A
Altitude	0-90 kft. AGL
Size	1 ft. x 1 ft. x 1 ft.
Payload Capacity	< 5 lbs.
Power	USB Battery Pack
Platform Cost	$10
Recurring Cost	~$300/flight

Launch services provided by Edge of Space Sciences: www.eoss.org

UAS Overview: Common Avionics

- Pixhawk autopilot and uBlox GPS
  - $290 for both
- PX4 firmware stack
- Provides blended navigation solution
- Wide variety of platforms supported
- Several built-in flight control modes
- ROS or mavlink libraries used for interfacing
- Subscribe to:
  - GPS with QoS
  - Orientation in Euler angles or Quaternions
  - Local position estimates

Image from: www.pixhawk.org

Constrained SWaP Hardware

- Each platform has constraints on the size, weight, and power of equipment it can support (SWaP)
- Power provided by modern LiPo batteries is abundant
  - AlienBee battery provides >300 W
- Space for electronics integration is limited
- Payload weight is extremely limited
  - Additional payload directly impacts flight time/range

SDR Hardware

Radio Front End

- Frequency Conversion
- Conditioning
- Data conversion

Programmable Logic

- Custom logic circuits
- Low latency
- Highly parallel
- Limited memory
- Rigidly defined
- Long compile times

General Purpose Processor

- Flexible software
- Open-source tools
- Fast clocks
- Access to RAM and HD
- Networked

Physical Connection

High Speed Bus

Network Connection

SDR Hardware Implications

- Power limitations preclude the sustained use of high power amplifiers for transmission
- Size and weight restrictions limit the choice of processing hardware
  - PCIe cards and ATX motherboards are too bulky
  - GPUs are typically too heavy
- Embedded single-board-computers (SBCs) are small enough
- FPGAs are small and highly efficient
  - Leverage the existing programmable logic in the SDR architecture

Historical Embedded Limitations

- SBCs have historically suffered from:
  - Low performance CPUs
    -> Limits proc. rate
  - Small amount of RAM
    -> Limits buffer sizes
- Slow interfaces (USB 2.0, UART)
  -> Limits radio peripheral data rates
- Slow memory hardware (SD cards)
  -> Limits full rate data recording

Enabling Technologies

- **Smart phones**
  - Faster, multi-core CPUs
  - More RAM
  - High performance interface support
  - Wide bandwidth memory support
- **FPGAs and Moore's law**
  - Faster, cheaper, smaller
- **System-on-chips**
  - Integrates FPGA/CPU
  - Reduces package size
  - High rate data interface
- **Radio-on-chips (RF ICs)**
  - Ultra-low SWaP

Processing Hierarchy

- Hierarchy of processing established to address SWaP constrained challenges
- Increasing algorithm maturity
- Increasing on-board processing
- Increasing development time/effort
- Decreasing flexibility

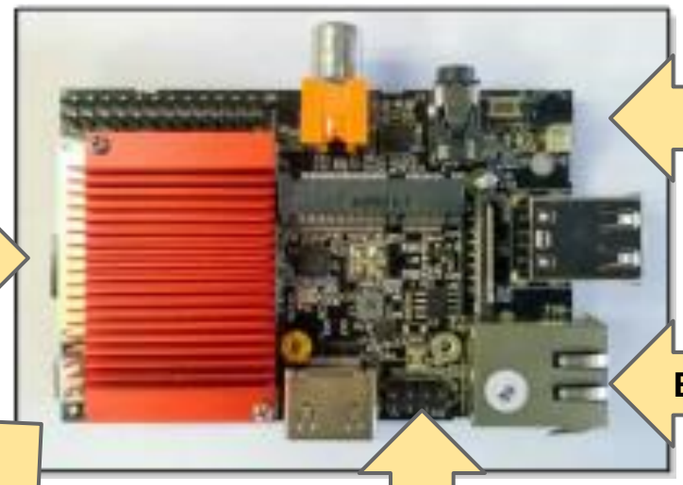
Processing Hierarchy

1. Data Recorder
    a. Low performance CPU
    b. High rate memory interface
    c. No guidance feedback
    d. Ideal for algorithm development
    e. Processing is all off-line
    f. Fly, record, land, process, update

Processing Packages: Data Recorder

HackRF One Radio

HummingBoard SBC



USB 2.0

WiFi

Used in field deployment

Ethernet

Used for data offloading

USB 2.0

MSata

256 GB SSD

rtl-SDR

Image from: www.mathworks.com

Processing Packages: Data Recorder

CPU Cores	CPU Clock	Interfaces	RAM	Memory
2	1.2 GHz	USB 2.0, Ethernet, mPCIe	1 GB	32 GB SD, 256 GB SSD

FPGA Name	FPGA Cells	FPGA BRAM	FPGA Multipliers
N/A	N/A	N/A	N/A

Radio Name	Channels	Duplex	IBW	Freq. Range	Bits	Interface
HackRF	1 Rx/TX	Half	<20 MSPS	1 MHz - 6 GHz	8	USB 2.0
rtl-SDR	1 Rx	N/A	<2.4 MSPS	24 MHz-1766 MHz	8	USB 2.0

Size	Weight	Power	Cost
3.1" x 4.9" x 1.6"	0.39 lbs.	6.5 W	$475

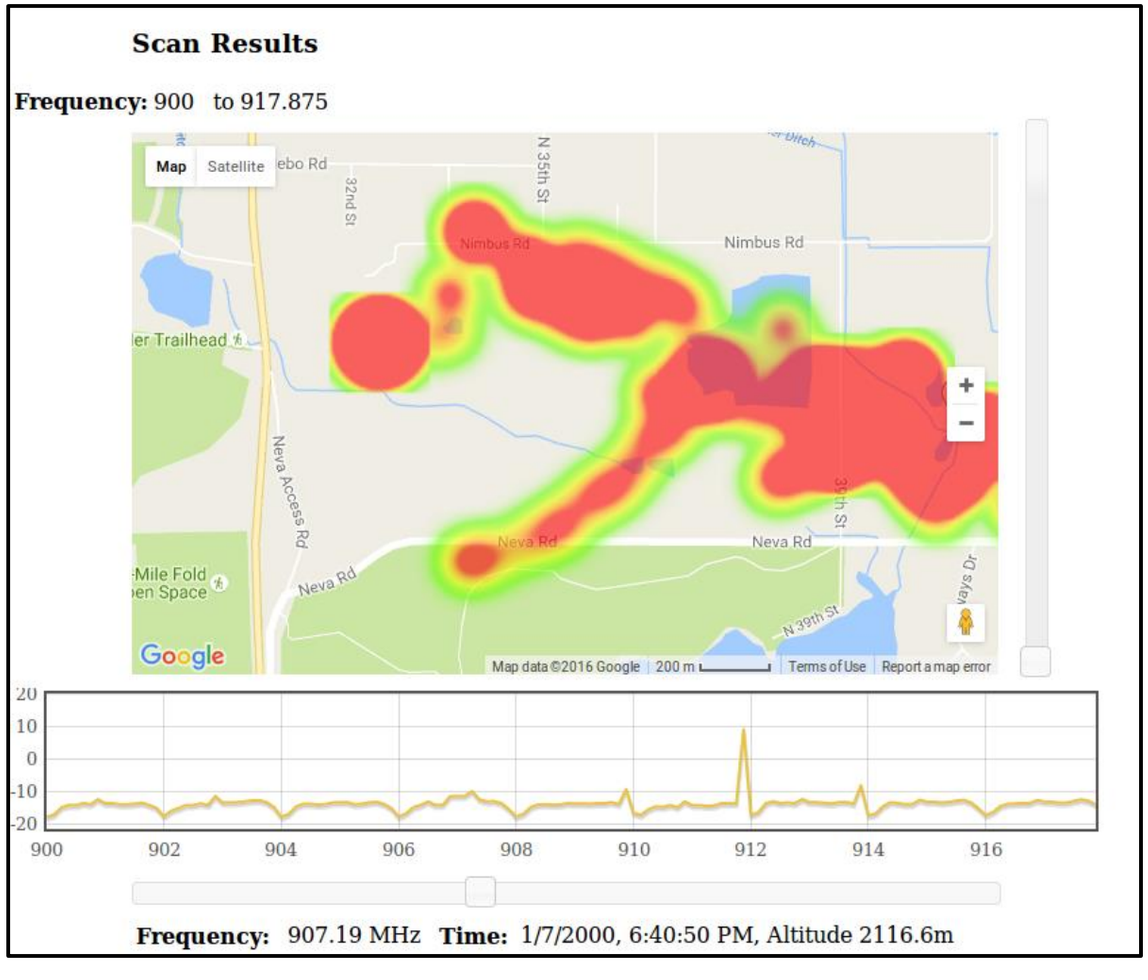
Processing Packages: Data Recorder

- Separate IQ data and metadata recording
- Take metadata with ROS or library plug-ins
- User Google protocol buffers for metadata
  - Time-stamp
  - Radio state
  - GPS
  - Local position estimate
  - Orientation
  - Air-data
  - File-name, offset, size
- IQ Data is large
  - 8 bits @ 2 MSPS => 3.8 MB/s
  - 16 bits @ 20 MSPS => 76 MB/s
  - 2x 16 bits @60 MSPS => 458 MB/s
- Protobuf metadata is used to index
  - Raw parsing
  - SQLite database
- Avahi networking is used to connect data recorder to ground-station in the field
- Ethernet is prefered for data transfers in the lab

Processing Packages: Data Recorder

- Initial version of data recorder was integrated with DJi Phantom 2
- rtl-SDR radio was integrated
  - Directional log-periodic antenna
- GPS only

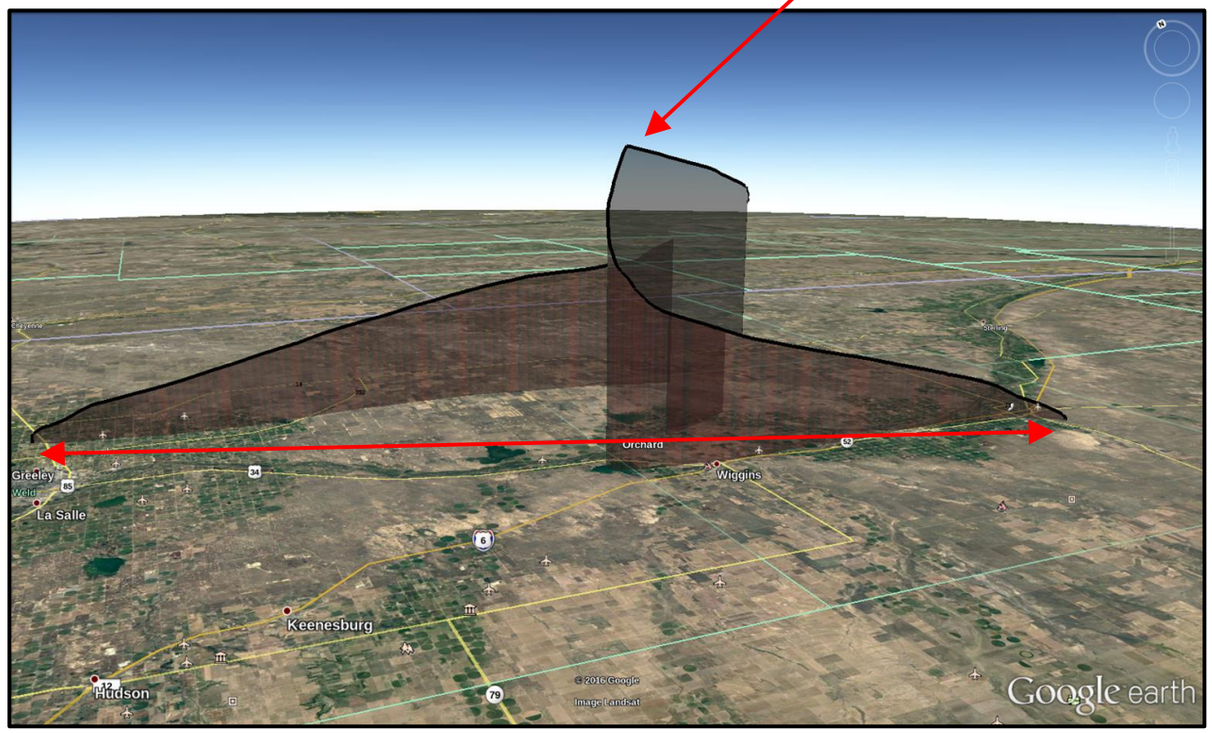
- HD could record ~16 hours of IQ data at 2.4 MSPS
- Circular flight plan was executed
- Altitude varying flight plan was executed
  - Leverage variation in el. patterns
- GPS tagged results were used to generate heat-maps
  - User visualization
  - Coverage maps
  - Emitter Localization



Processing Packages: Data Recorder

- Lessons learned from first flight were adapted, package was upgraded
- Two packages were integrated into a weather balloon
  - HackRF radios
  - One duck antenna, one log-period
- One package scanned TV bands
  - Looking to estimate HDTV antenna elevation patterns
- One package linearly scanned through bands
- Pixhawk with PX4 was integrated
  - ROS used for integration
- Protobufs included in data recording
- HDTV package could record IQ data for ~6 hours at 6 MSPS
- Scanning package could record IQ data for ~4 hours at 10 MSPS

94,000 ft apogee

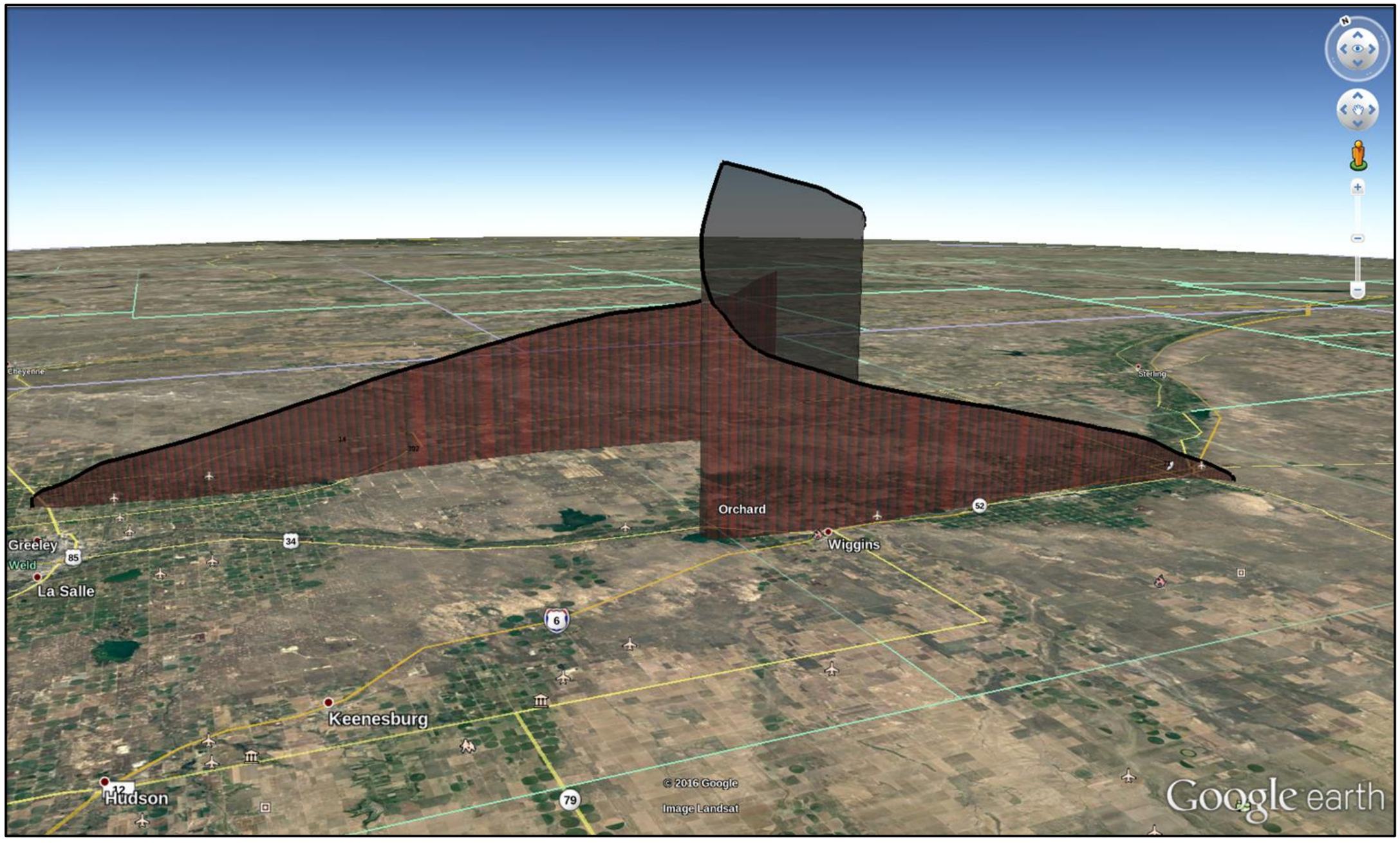


~63 mile cross-range drift

Our github for this project: github.com/dirkcgrunwald/ros-sdr

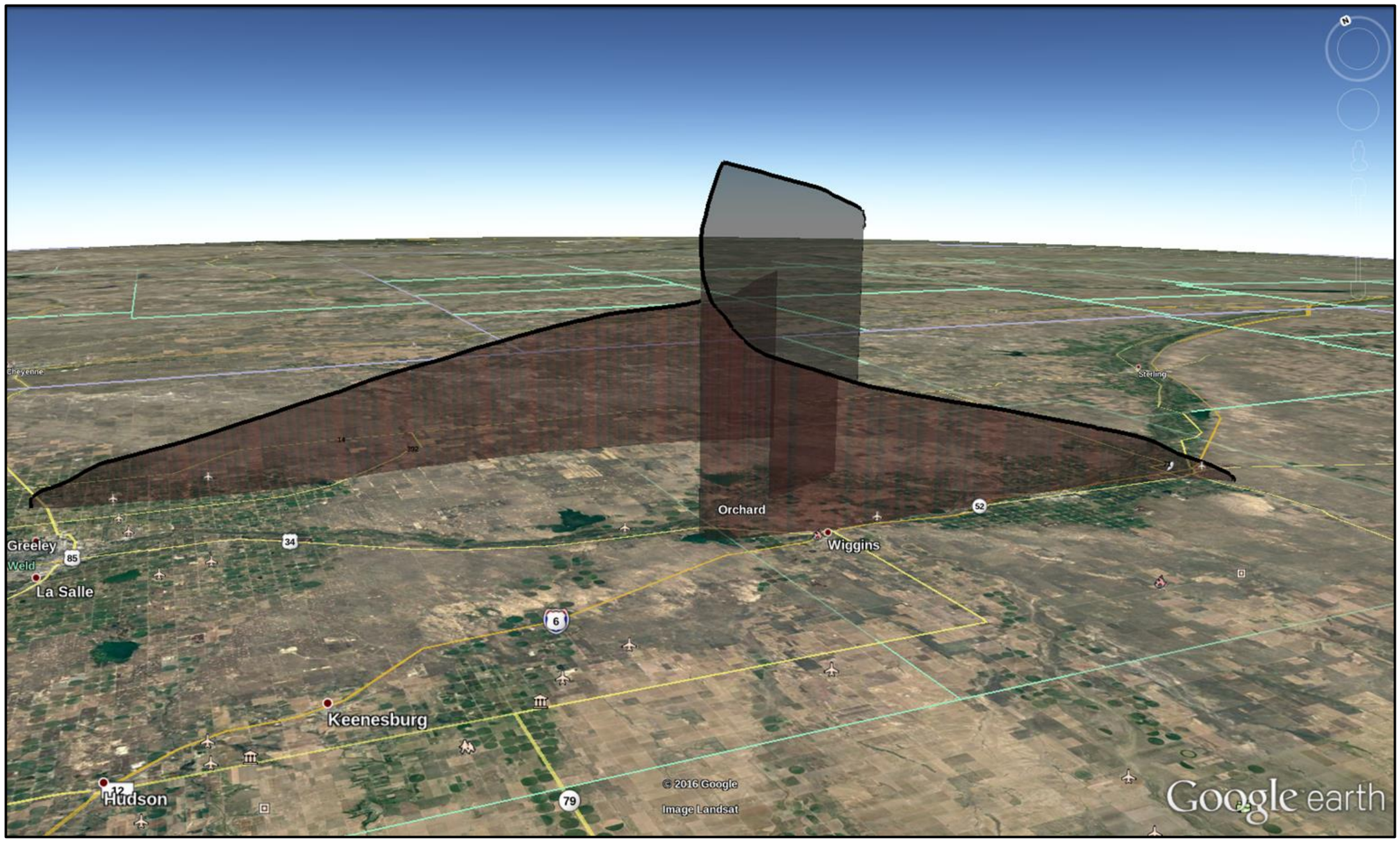
Processing Packages: Data Recorder

617 MHz



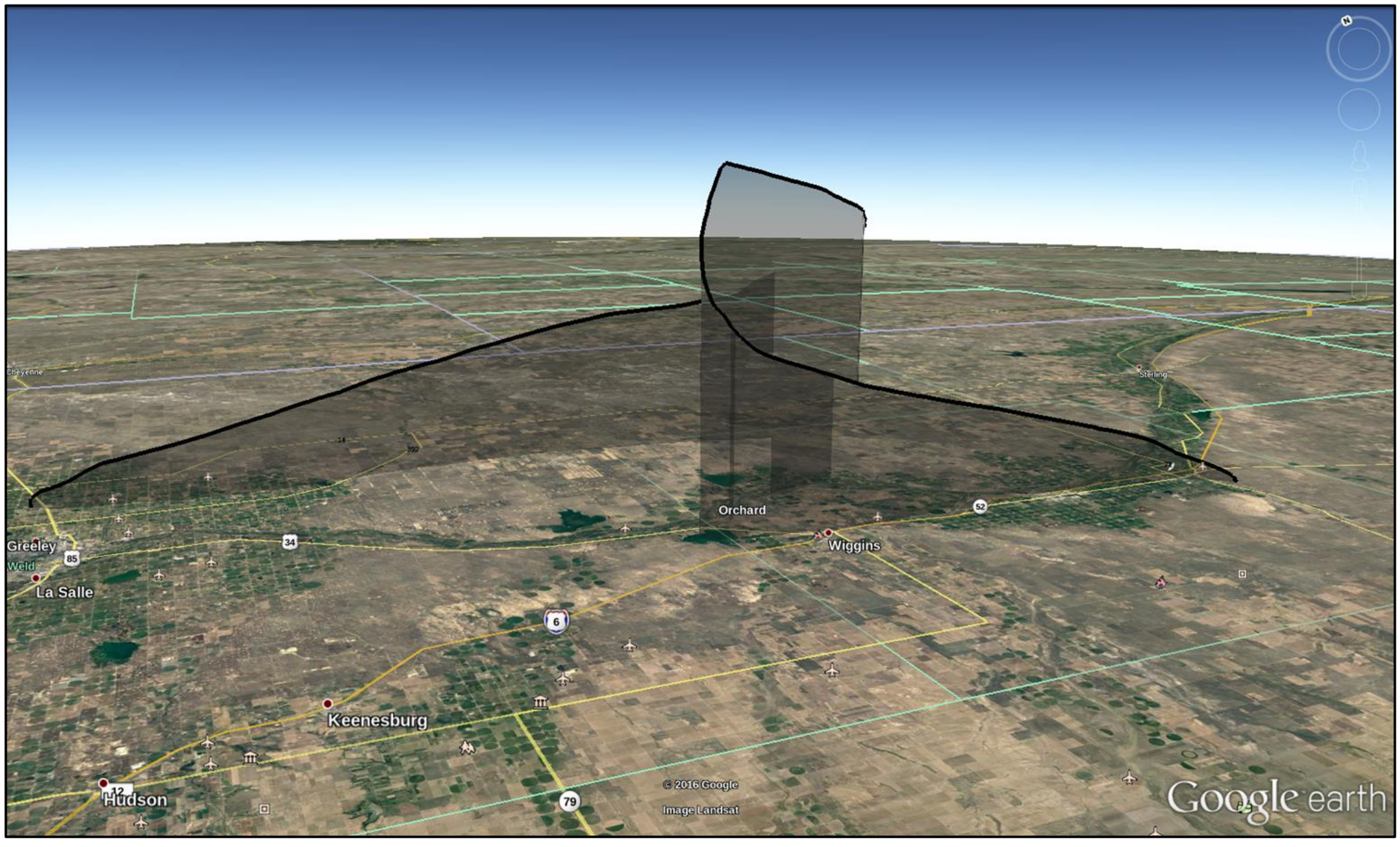
Processing Packages: Data Recorder

515 MHz



Processing Packages: Data Recorder

549 MHz

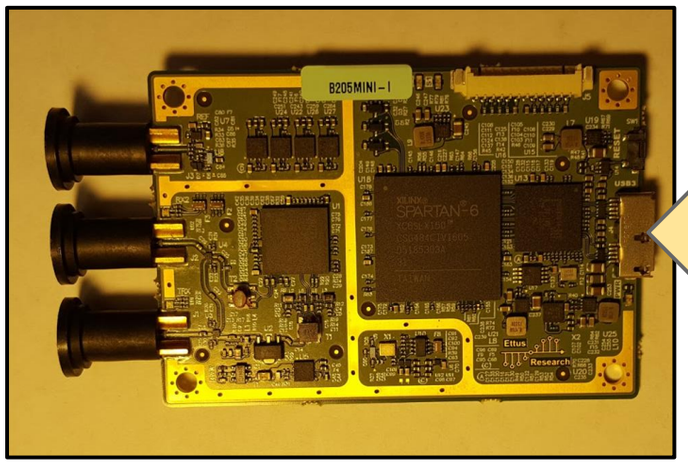


Processing Hierarchy

2. Onboard CPU Processing
    a. High performance CPU
    b. High rate interfaces
    c. Guidance feedback possible
    d. Somewhat mature algorithms
    e. Processing can be distributed
    f. Software keeps it flexible
    g. Design algorithms for low processing

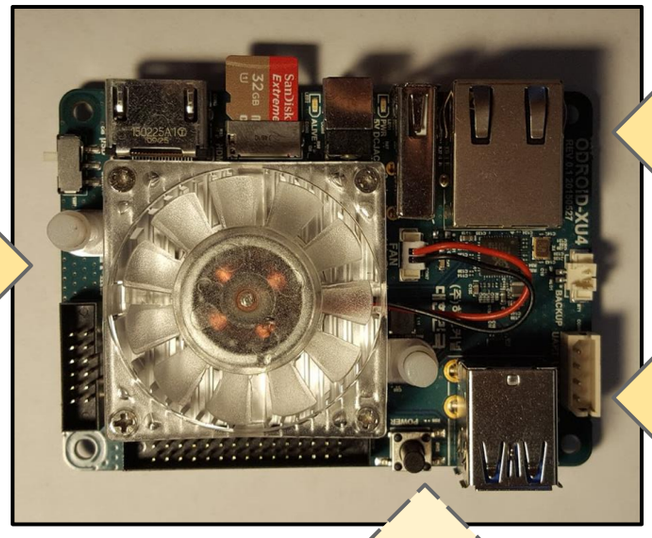
Processing Packages: Onboard CPU Processing

Ettus B205mini



USB 3.0

ODroid XU4



WiFi

Used in field deployment

Ethernet

Used for data offloading

USB 3.0

128 GB SSD

Processing Packages: Onboard CPU Processing

CPU Cores	CPU Clock	Interfaces	RAM	Memory
8	2 GHz	USB 2.0, USB 3.0, Ethernet	2 GB	32 GB SD, 64 GB eMMC

FPGA Name	FPGA Cells	FPGA BRAM	FPGA Multipliers
Spartan 6 LX150	147k	4824 Kb	180

Radio Name	Channels	Duplex	IBW	Freq. Range	Bits	Interface
AD9364	1 Rx/TX	Full	<~30 MSPS	70 MHz - 6 GHz	12	USB 3.0

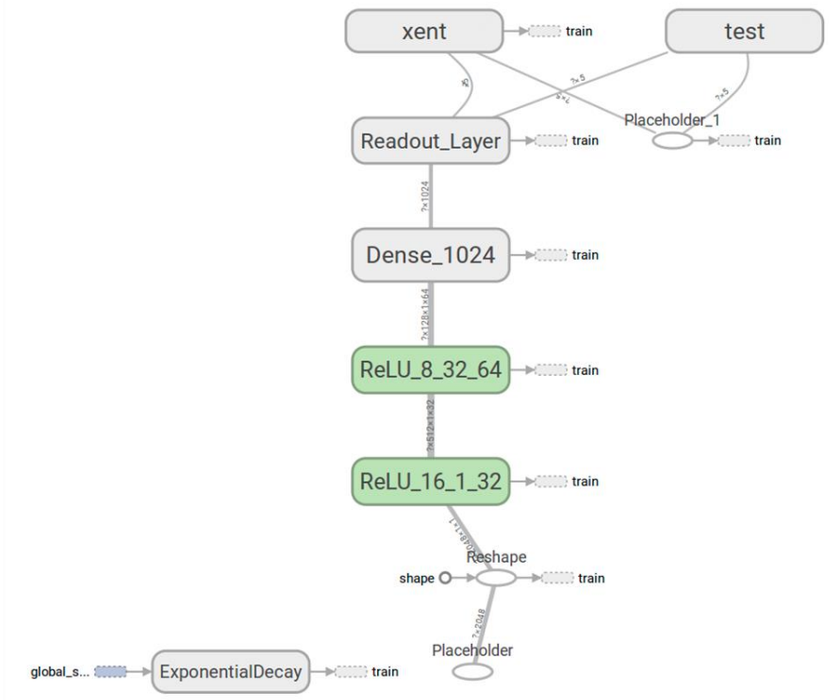
Size	Weight	Power	Cost
2.3” x 3.5" x 2"	0.23 lbs.	<23 W	$889

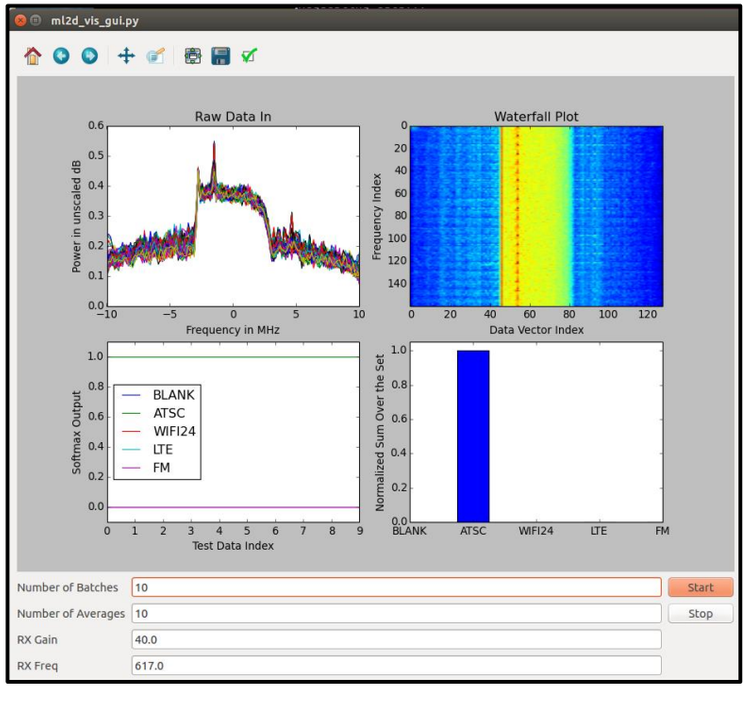
Processing Packages: Onboard CPU Processing

- Lessons learned adopted
- Port selection is important
  - USB 3.0 shared by radio, Ethernet, and SSD
  - Near continuous data recording
    - Buffer to bigger RAM
    - Write to eMMC/SSD
- No GNU Radio or ROS
  - Development overhead
  - More flexibility without
  - Adapt principles
- Choose the right language
  - Fast processing in C++
  - Complicated code in python
  - Protobufs for compatibility
  - Processing integrated with ZMQ
    - Efficient and distributable
- Design algorithm to minimize processing
  - Log2 vs. Log10
  - Running max holds

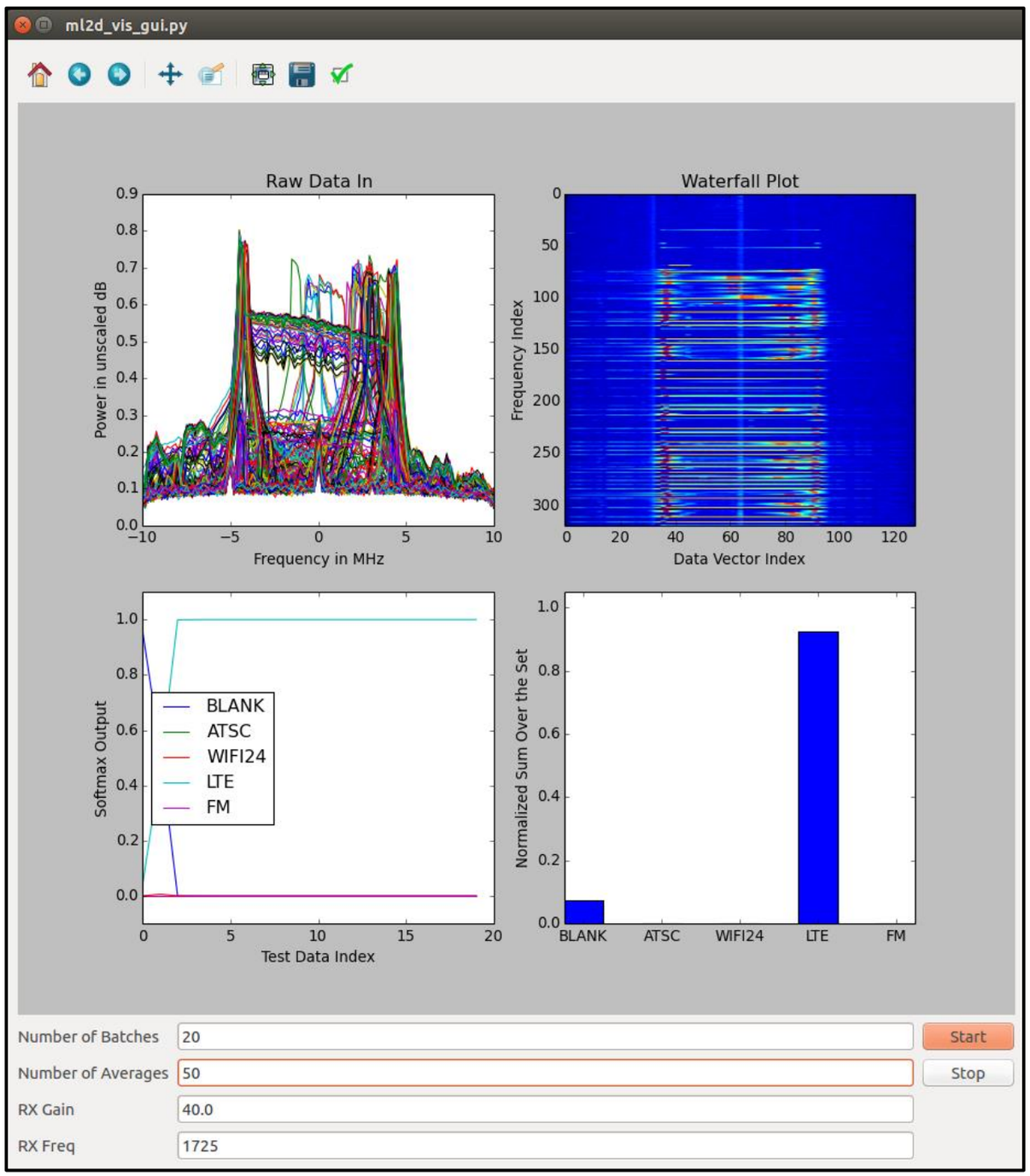
Processing Packages: Onboard CPU Processing

- Signal identification application was developed
- Frequency-domain detection of PSD envelope using deep learning techniques
- Max-hold reduces data rate and maintains privacy
- Wideband data is collected in frequency and time
- Feeds trained 2D CNN
- CNN produces probability of label
- Front end, CNN, and visualization can be distributed





Processing Packages: Onboard CPU Processing



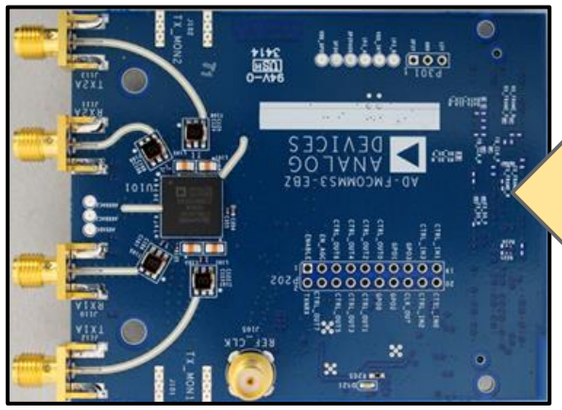
Git repo: bitbucket.org/austinsteamboat/cnn_sdr_specmon

Processing Hierarchy

3. Onboard FPGA Acceleration
    a. Host bulk of DSP on FPGA
    b. CPU for management
    c. Guidance feedback possible
    d. Very mature algorithms
    e. Firmware is rigidly designed
    f. Design algorithms for full-rate processing

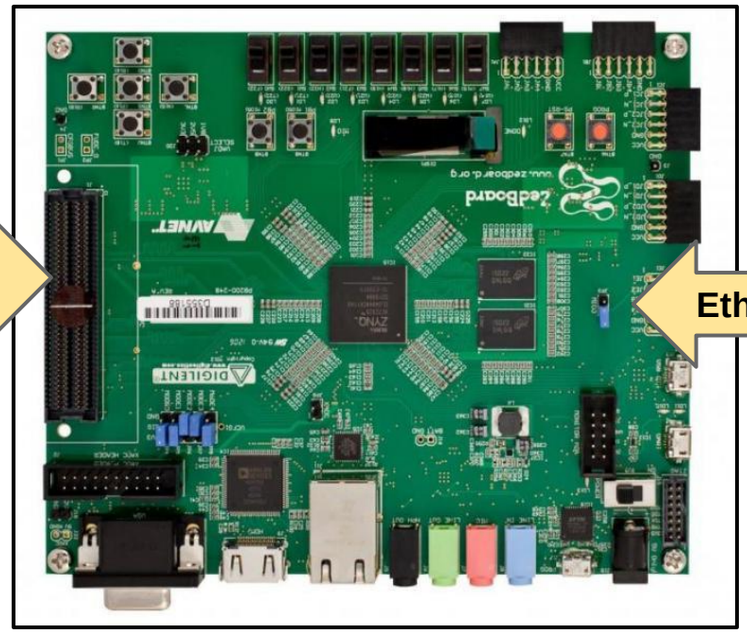
Processing Packages: Onboard FPGA Acceleration

FMCOMMS3



FMC

Zedboard



Ethernet

Used for data offloading

FMCOMMS Image from: www.analog.com
Zedboard Image from: www.zedboard.org

Processing Packages: Onboard FPGA Acceleration

CPU Cores	CPU Clock	Interfaces	RAM	Memory
2	667 MHz	USB 2.0, Ethernet	512 MB	32 GB SD

FPGA Name	FPGA Cells	FPGA BRAM	FPGA Multipliers
Zynq 7Z020	85k	4480 Kb	220

Radio Name	Channels	Duplex	IBW	Freq. Range	Bits	Interface
AD9361	2 Rx/TX	Full	2-61.44 MSPS (56 MHz max)	70 MHz - 6 GHz	12	FMC

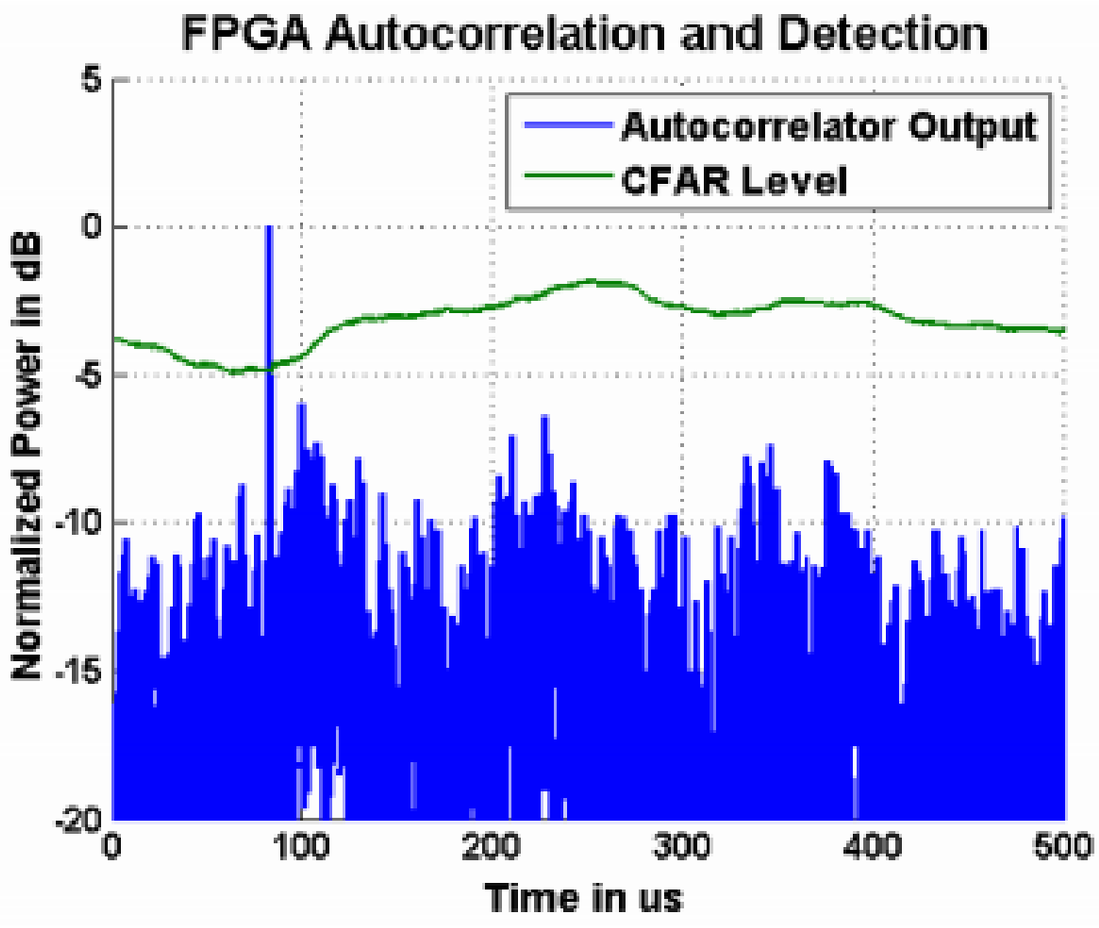
Size	Weight	Power	Cost
5.3” x 9.4" x 0.9"	0.43 lbs.	7 W	$1069

Processing Packages: Onboard FPGA Acceleration

- SoCs result in very small packages
- Tight integration of CPU/FPGA simplifies high-rate data interface
  - Zedboard has slow CPU, big FPGA
    - Host bulk of DSP in firmware
    - Let CPU manage
  - Data is preprocessed to significantly reduce rate exposed to CPU
- Focus on developing modular, open-source designs
  - Improves design reusability
  - Easier for porting
  - Network-on-Chip (NoC) architecture
    - Simplifies integration
    - Improves versatility of FPGA
  - Automated Build tools
    - Reduces challenge of tool compatibility

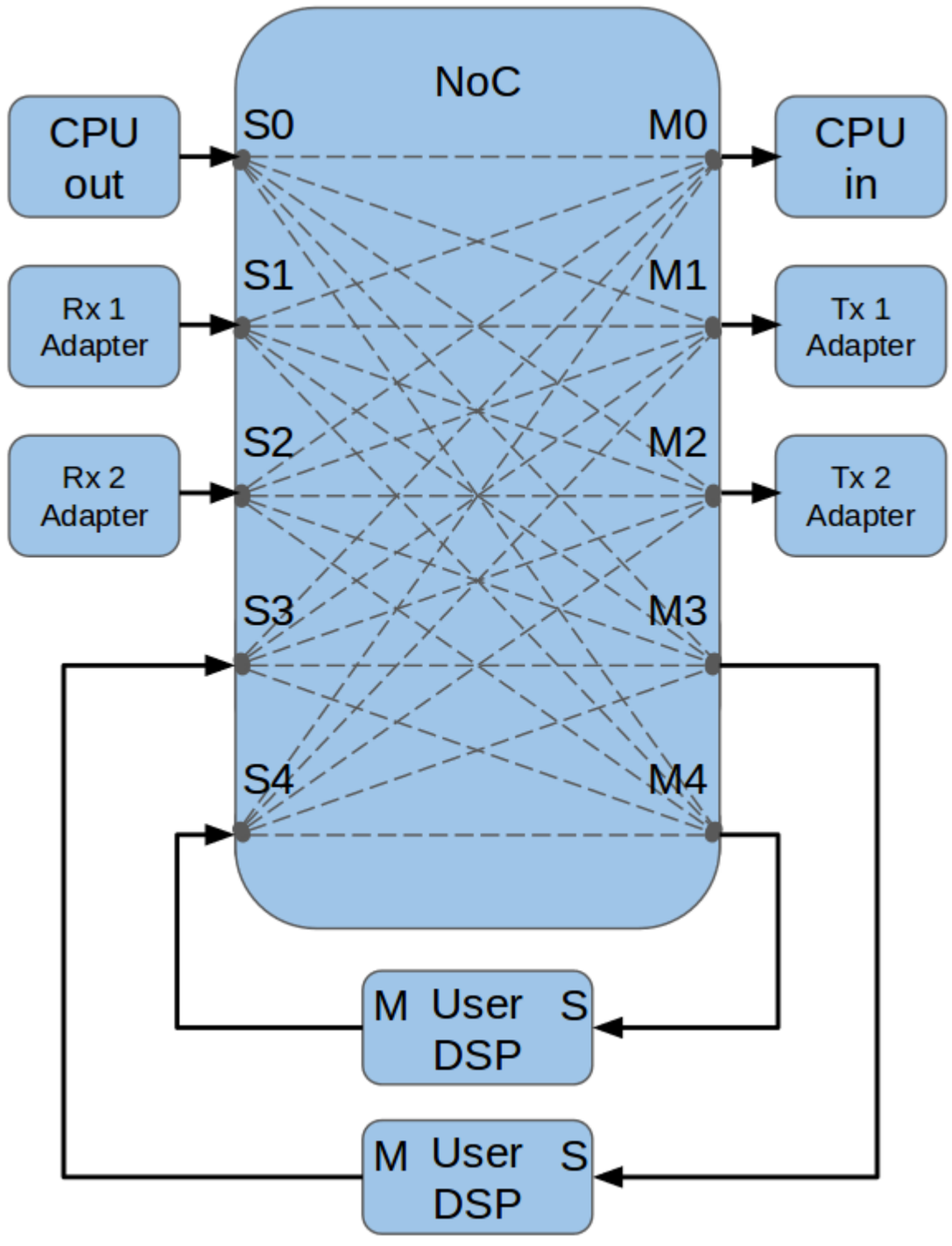
Processing Packages: Onboard FPGA Acceleration

- Satellite navigation project at CU researching using signals of opportunity
- Extract timing from GPS disciplined ATSC signal
- FPGA design to:
  - Apply complex auto-correlation
  - Detect resulting peaks
  - Report power and timing of peaks
- Modular components were developed and implemented
- Reduces data rate from 23 MB/s to 0.48 KB/s
  - 50000x reduction in data rate



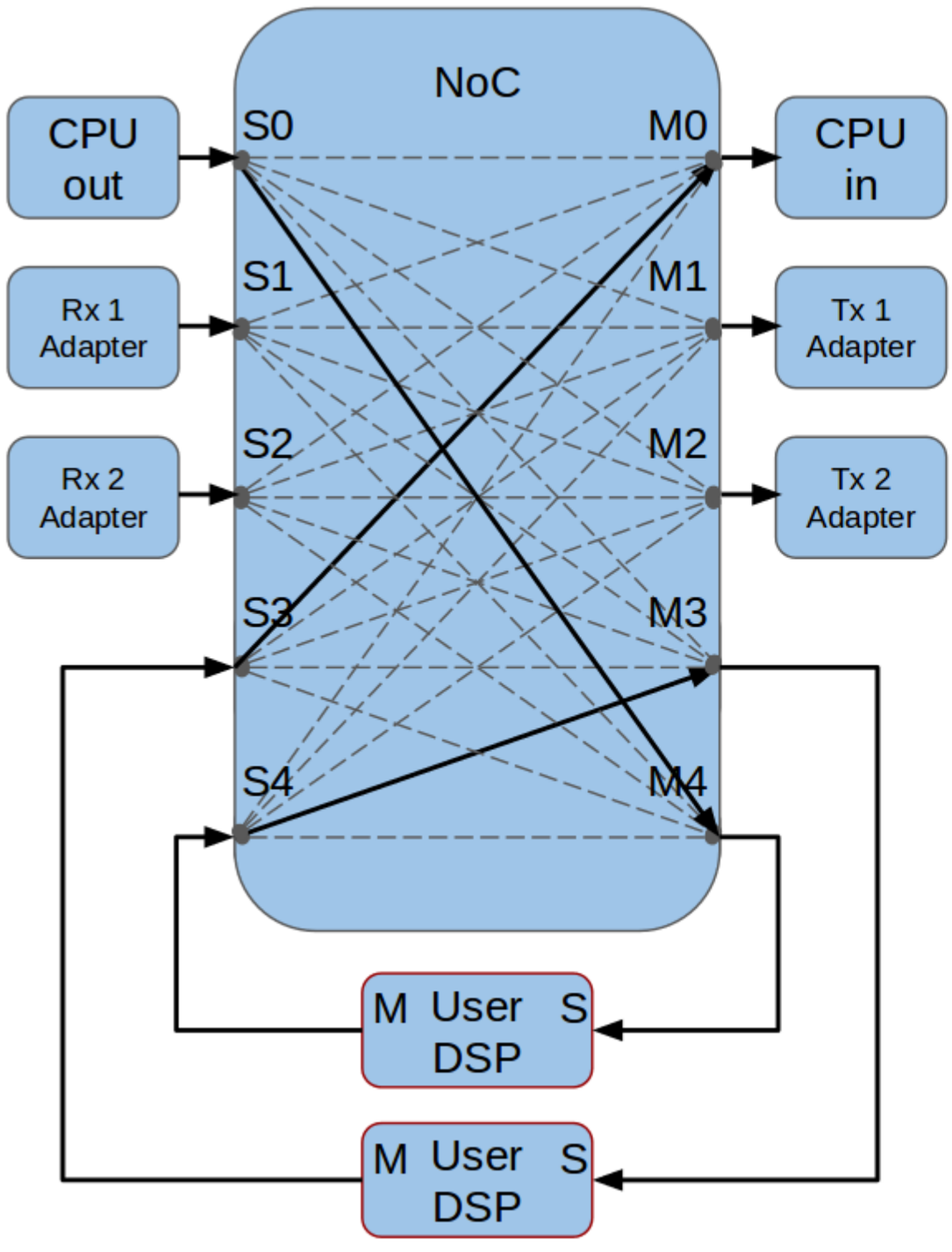
Processing Packages: Onboard FPGA Acceleration

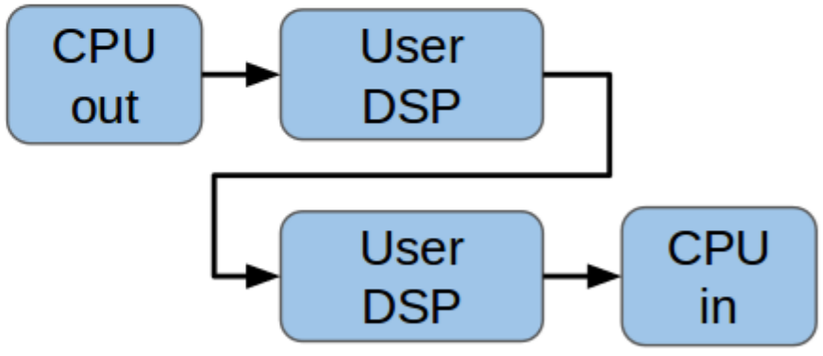
- NoC architecture developed
- Standard interfaces
- Reconfigure processing chain
- AXI-4 stream and cross-bar switch
  - Simple
  - Widely compatible
- Supports asynchronous designs
- Automated build process for integrating computing elements
  - Uses python scripting for VHDL and TCL script generation
  - Uses Docker for tool stability
  - Launching as a web service



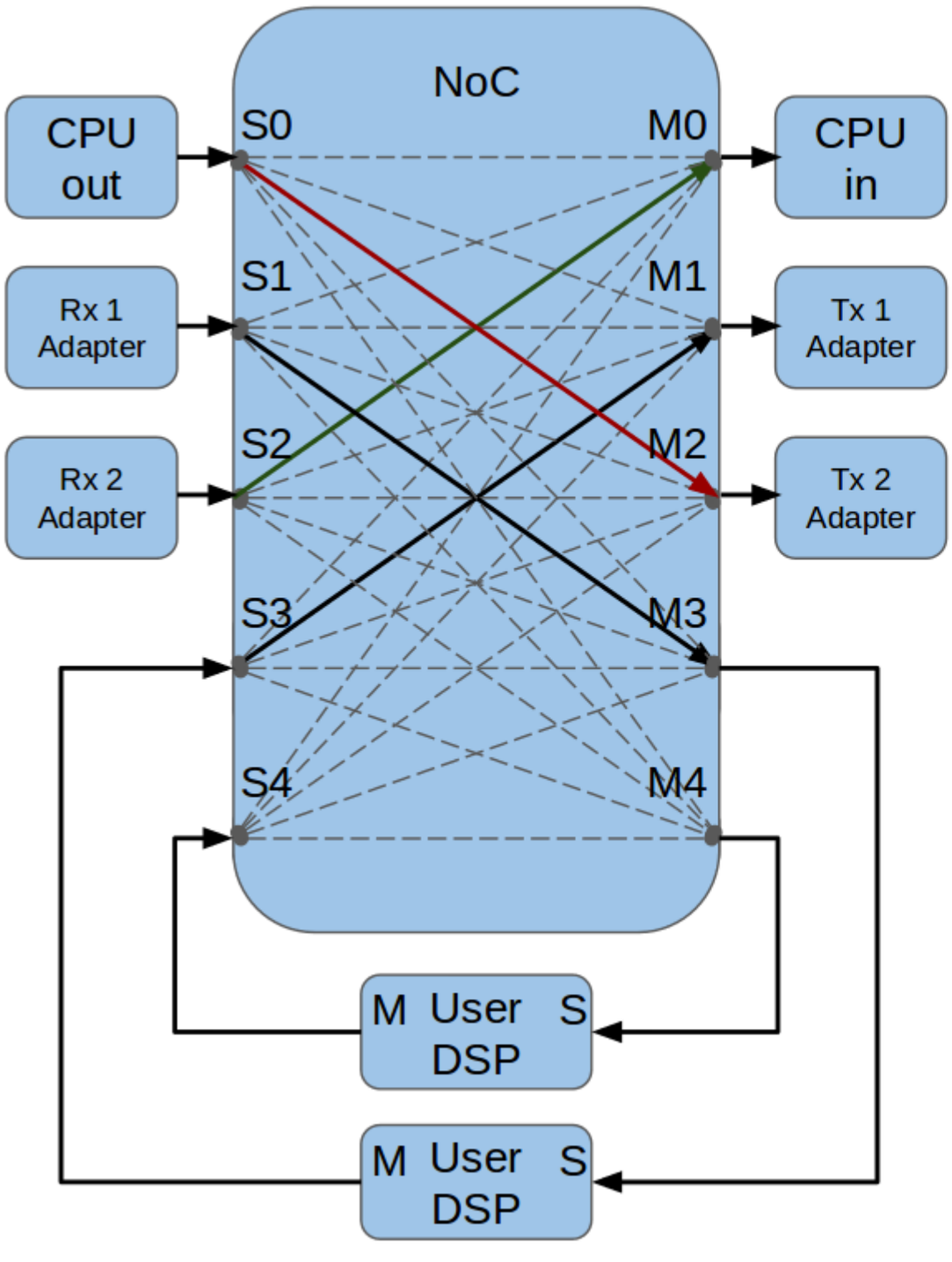
Git Repo: bitbucket.org/cusdr/cunoc_sdr/wiki/Home

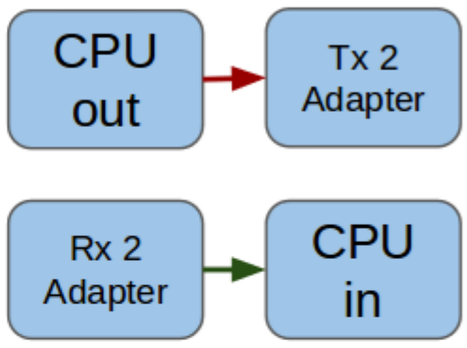
Processing Packages: Onboard FPGA Acceleration





Processing Packages: Onboard FPGA Acceleration



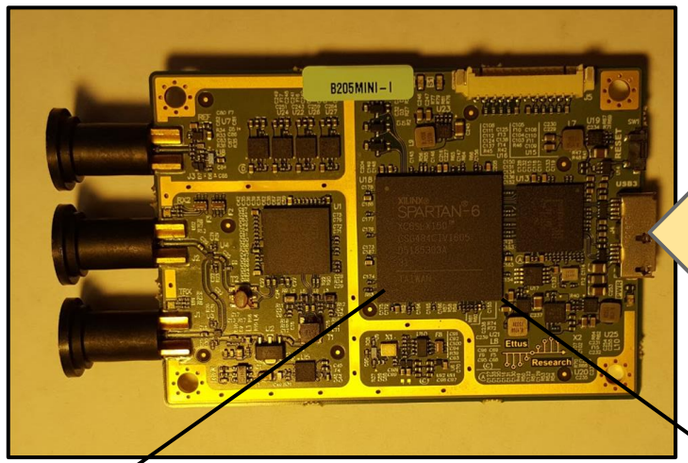


Going Forward

- Separate CPU/FPGA
  - Fully leverage advances in embedded CPUs
- Focus on widely used OS with package manager
  - Software installation is a major challenge
  - The more its used, the more bugs are worked out
- Start flying more
  - New FAA regulations are far friendlier

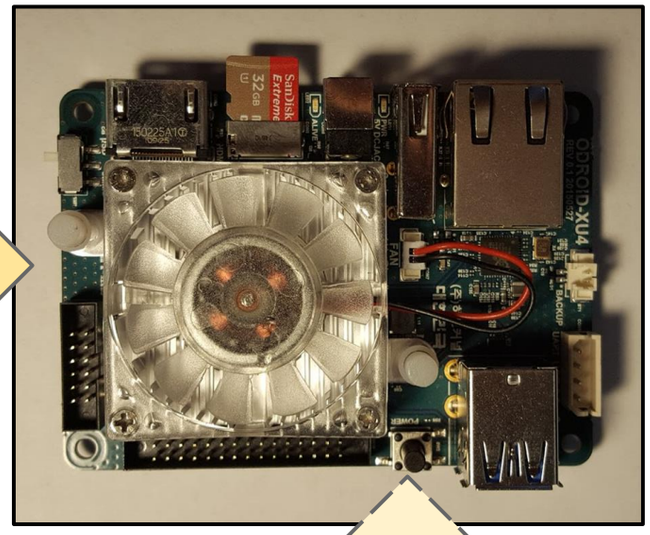
Going Forward

Ettus B205mini

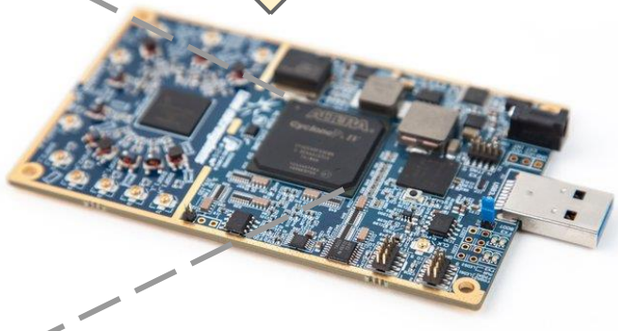


USB 3.0

ODroid XU4



USB 3.0



LimeSDR

USRP 3: B205 Firmware

User Firmware

Data In
Enable
Reset
IP
Data Out

Radio Phy

Data Framing

USB 3.0 Phy

Sprite Drone

Modular Payload Bay

LimeSDR Image from: www.crowdsupply.com/lime-micro/limesdr
Sprite Image from: www.ascentaerosystems.com

Conclusion

- UAS are cost effective and practical
- UAS mobility improves spectrum monitoring performance
- SWaP drives hardware
- Embedded processors are getting better
- Hardware acceleration improves performance
  - Critical for full-rate processing
- Metadata database accelerates post-processing
- Design of efficient algorithms enables on-board processing
- Widely used SBCs reduce software development risks
- Separate FPGA and CPU improves flexibility
- FPGA development time can be reduced with NoC architecture

Acknowledgements

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- Jorge Cervantes - CU CCAR, ATSC Navigation Research
- Donald Kuettel III - CU CCAR, ATSC Navigation Research
- Dr. Denis Akos – CU CCAR, GPS Interference Research

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Questions?

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Backups

UAS Overview: Aerostat

Advantages

- Extremely long endurance
- Capable of lifting large, heavy payloads
- Very few regulations

Disadvantages

- No control
- Anchored in place
- Helium refills can be expensive over time
- Sensitive to inclement weather

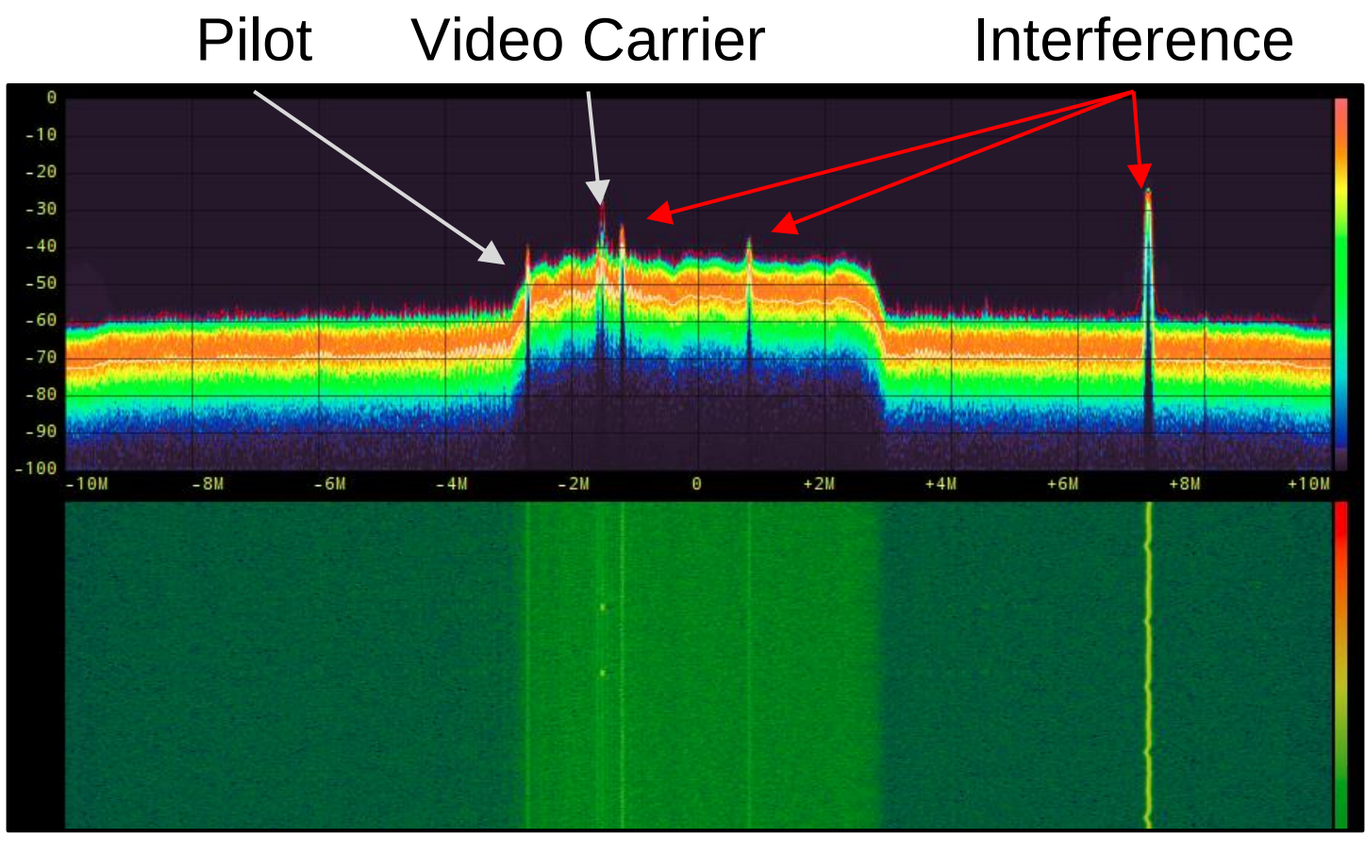
UAS Overview: Aerostat

Image from: www.advertising-balloons.com

Endurance	Days
Cruising Speed	N/A
Range	Tethered
Altitude	0-165 ft. AGL
Size	20 ft. long, 700 cubic feet
Payload Capacity	14 lbs.
Power	LiPo
Platform Cost	$1600
Recurring Cost	>$100/flight

Motivating Case Study

- Interference detected in ATSC band during machine learning collections
- Source is narrow-band
- Intermittent in time
- Powerful
- Found to be TV white-space microphones
  - Used by distance learning courses at CU



Motivating Case Study

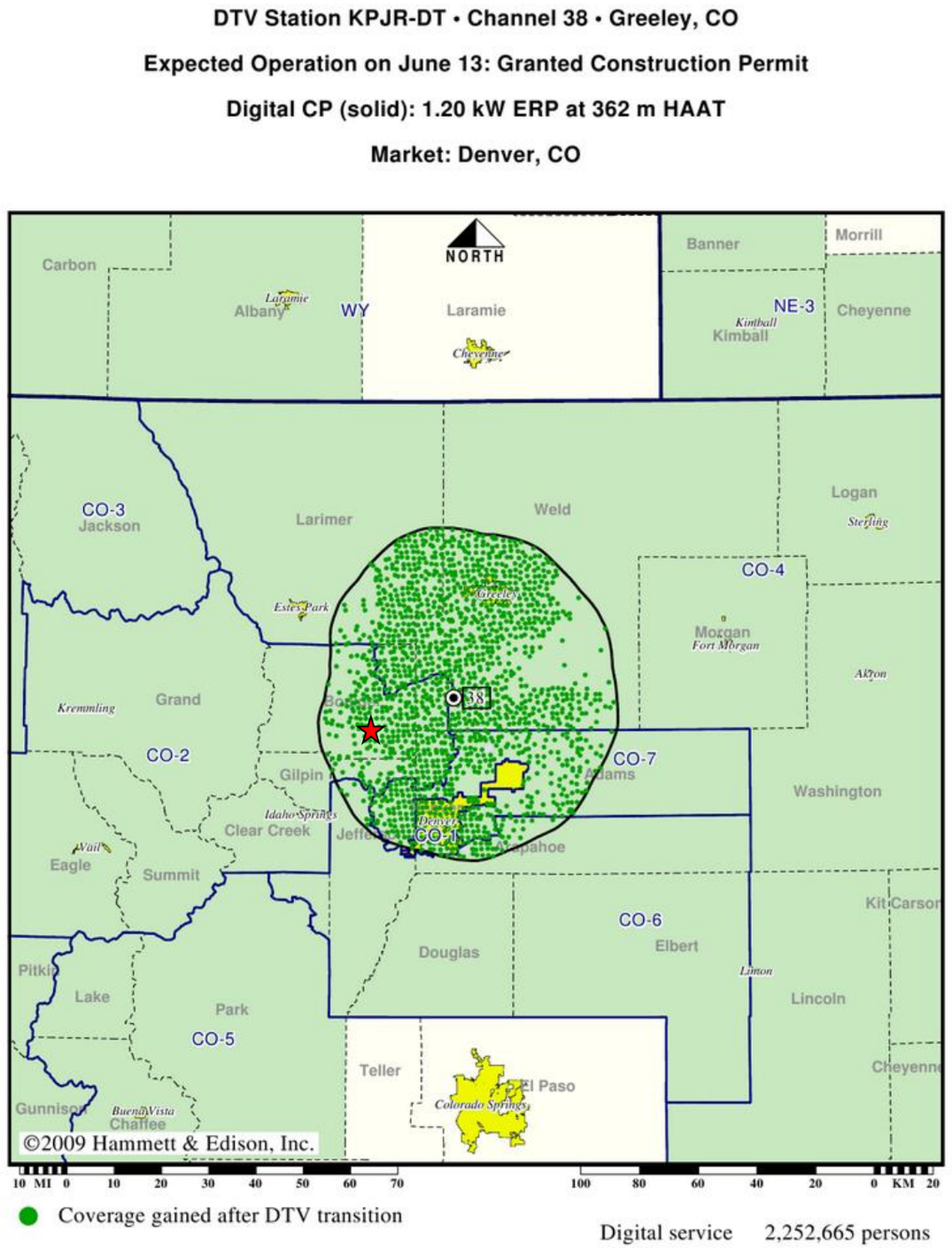


Image from: www.fcc.gov

Motivating Case Study

Enter your device type and location below

○ Fixed TVBD ○ Personal/Portable TVBD ◉ Wireless Microphone

CU Boulder [Search]

Best match:University of Colorado, CO

View Full Map

Channel Number	Frequency Range (MHz)	Availability	Noise Floor (dBm)
33	584-590	Reserved	**
39	620-626	Reserved	**
8	180-186	Available	**
10	192-198	Available	**
12	204-210	Available	**
14	470-476	Available	**
20	506-512	Available	**
2	54-60	White Space	**
21	512-518	White Space	**
22	518-524	White Space	**
23	524-530	White Space	**
25	536-542	White Space	**
28	554-560	White Space	**
30	566-572	White Space	**
42	638-644	White Space	**
44	650-656	White Space	**
47	668-674	White Space	**
49	680-686	White Space	**
50	686-692	White Space	**
51	692-698	White Space	**

No instruction for channel 38

Motivating Case Study

Motivating Case Study

- Localized, intermittent interference
  - Challenging for manual discovery
  - Well suited for automated UAS
- Interference source is asymmetric
  - Strong incentive for incumbent to take action
- FCC mapping provides insufficient guidance
  - Automated UAS can rapidly generate accurate, up-to-date radio maps